DATARAM CORPORATION

Book for
H2-197

SK 25105

PRINCETON-HIGHTSTOWN ROAD

CRANBURY, NEW JERSEY 08512

DR-111
MEMORY SYSTEM
INSTALLATION MANUAL

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1.0 GENERAL INSTALLATION PROCEDURE

1.1 Introduction

Dataram Corporation's DR-111 memory system can be installed into various models of the PDP-11* series computers, which are:

PDP-11/05
PDP-11/10
PDP-11/15
PDP-11/20
PDP-11/35
PDP-11/40
PDP-11/45
ME11-L Expansion Unit
MF11-L Assembly Unit

In general, the DR-111 memory system is inserted into the appropriate connectors so that the A and B plugs interface with the UNIBUS* connectors. The component side of the DR-111 electronics board faces the same direction as the component side of the standard PDP-11 circuit boards. The DR-111 stack board, which is plugged into the rear of the DR-111 electronics board, blocks the next connector slot.

The DR-111 memory system will not operate in the following configurations: ME11-LP, MF11-LP, MF11-U, MF11-UB, MF11-UC, MF11-UP, MF11-UR and MF11-US.

The ME11-LP and MF11-LP assembly and expansion units are wired for the MM11-LP memories. These systems are 8K x 18 parity units. The DR-111 is a 16 bit word system and does not have the two parity bits for this configuration.

The MF11-U series assembly units are wired for the MM11-U and MM11-UP 16K x 16 or 18 memory systems. These memory modules utilize supply voltages which are different from the voltages used by the DR-111 modules. The DR-111 will be damaged if it is plugged into these assembly units!

1.2 Unpacking and Inspection

Each DR-111 is shipped in an individual, foam-lined shipping container for protection. This container and black plastic wrapper should be saved for future use if the unit is returned for repair.

After unpacking the DR-111, it is important to inspect the unit for obvious physical damage prior to installation.

*PDP-11 and UNIBUS are registered trademarks of the Digital Equipment Corporation.

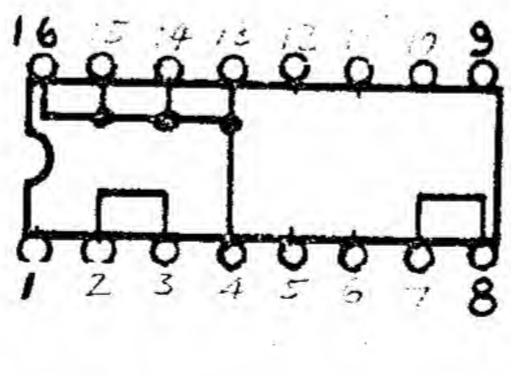
1.3 Address Strapping

Each memory module in a system must have a different block starting address to prevent more than one module from responding to the same address from the processor or DMA device. This is accomplished by "strapping" addresses A13 through A17 on each module via a 16-pin dual in-line strapping plug and socket and wire wrap jumpers. The initial address may be any of the following:

JUMPER LOCATIONS FOR MEMORY STRAPPING

Initial Address	From Pin 2 To	From Pin 7 To	From Pin 4 To		Wire Wrap Jumpers	
			8K	16K	R To	W To
0	3	8	16,15	16-13	P	V
4K	3	8	15,14	15-12	P	V
8K	3	8	14,13	14-11	P	V
12K	3	8	13,12	13-10	P	V
16K	3	8	12,11	12-9*	P	V
20K	3	8	11,10	11-9 & 5	U	V
24K	3	N/C	10,9*	15 & 10	P	U
32K	3	6	16,15	16-13	P	V
40K	3	6	14,13	14-11	P	V
48K	3	6	12,11	12-9	P	V
56K	3	N/C	10,9	9 & 5	P	U
64K	1	8	16,15	16-13	P	V
72K	1	8	14,13	14-11	P	V
80K	1	8	12,11	12-9	P	V
88K	1	N/C	10,9	15 & 10	P	U
96K	1	6	16,15	16-13	P	V
104K	1	6	14,13	14-11	P	V
112K	1	6	12,11	12-10	P	V (124K Max.)
120K	1	N/C	10	N/A	P	U

*Jumper T-S for 31K Operation



Plug shown for Initial Address of 0, 16K Memory System

1.4 Address Strapping DEC*MM11-L Memory System

When increasing the capacity of a PDP-11 computer, it may become necessary to remove one or more DEC MM11-L systems. For example, a PDP-11/05 with 16K of memory (two MM11-L systems) can be expanded to 24K by replacing one of the 8K MM11-L systems with a 16K DR-111 system.

As with the DR-111 system, the MM11-L systems are also "strapped" for different block starting addresses. For the given example, one module is strapped 0-8K and the other 8-16K.

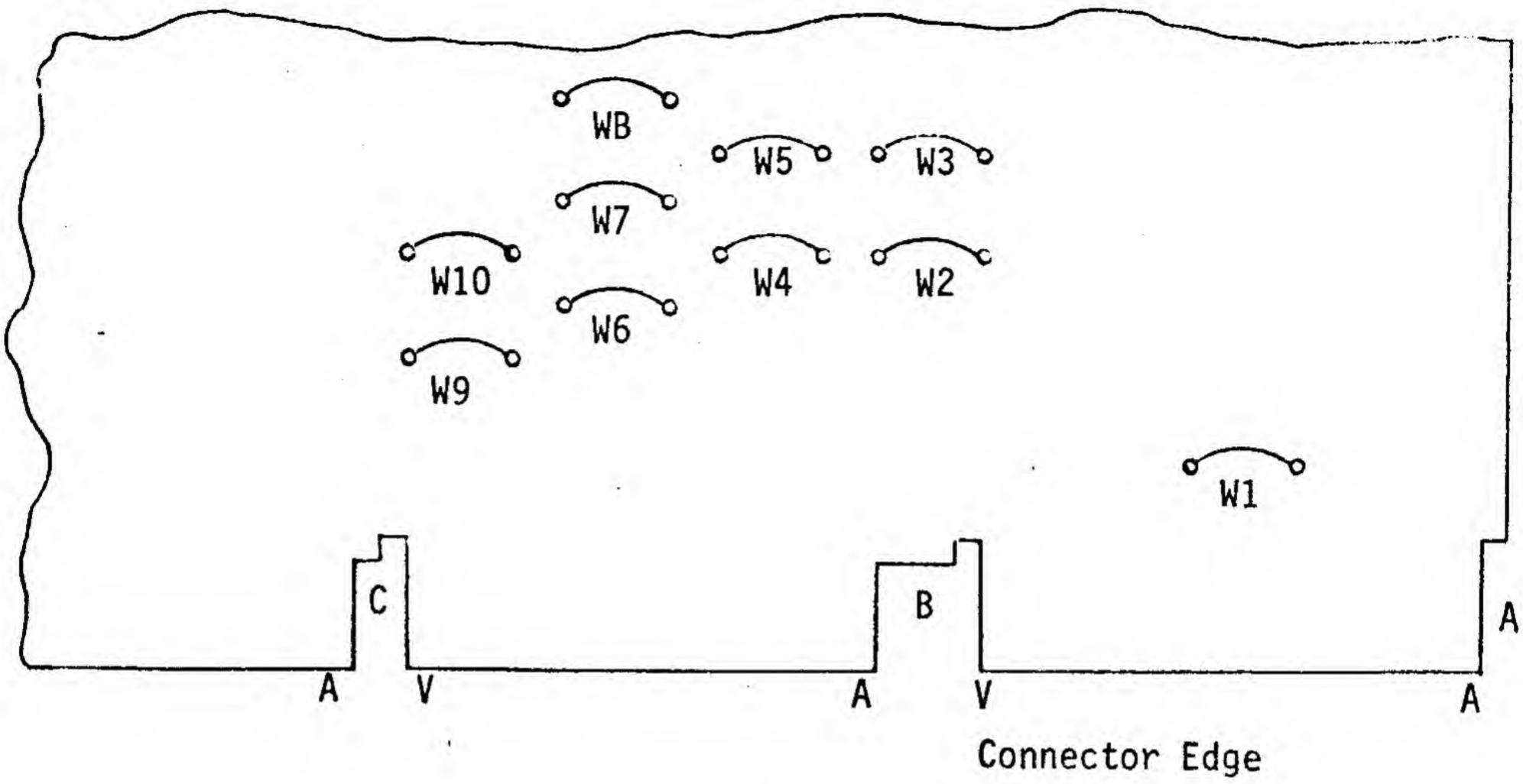
The modules strapped for 8-16K must be removed. This strapping, shown in Figure 1, is accomplished with four jumpers (W2, W3, W4 and W6) located on the G110 Control Module.

The MM11-L memory system consists of three modules: G110 Control Module, G231 Memory Driver Module, and H214 Memory Stack Module. All three modules must be removed when replacing an MM11-L with a DR-111.

*DEC is a registered trademark of Digital Equipment Corporation

CONTROL MODULE G110

Component Side



Jumper locations W1, W5, W9 and W10 are shown for reference only.

Memory Bank (words)	Device Address Jumpers W6 A14 or A01	W4 A15	W3 A16	W2 A17L
0-8K	In	In	In	In
8-16K	Out	In	In	In
16-24K	In	Out	In	In
24-32K	Out	Out	In	In
32-40K	In	In	Out	In
40-48K	Out	In	Out	In
48-56K	In	Out	Out	In
56-64K	Out	Out	Out	In
64-72K	In	In	In	Out
72-80K	Out	In	In	Out
80-88K	In	Out	In	Out
88-96K	Out	Out	In	Out
96-104K	In	In	Out	Out
104-112K	Out	In	Out	Out
112-120K	In	Out	Out	Out
120-128K	Out	Out	Out	Out

DEC ADDRESS STRAPPING
Figure 1

2.0 INSTALLATION IN PDP-11/05 and PDP-11/10

2.1 Standard DEC PDP-11/05 and PDP-11/10 Configurations

There are two configurations of the 5¼" PDP-11/05 and PDP-11/10 assembly units which are shown in Figure 2. The 10½" PDP-11/05 and PDP-11/10 assembly units have one configuration and this is shown in Figure 3.

Configuration 1 of the 5¼" unit is wired for 16K of DEC memory (6 boards) with one small peripheral controller slot.

Configuration 2 of the 5¼" assembly unit is wired for 8K of memory with four small peripheral controller slots.

The 10½" assembly unit is wired for 16K of memory. The computer chassis also has space available for 3 nine slot system units.

The DR-111 modules may be installed in various combinations with or without the MM11-L memories. No modification of the computer backplane is necessary. The following subsections describe typical memory configurations.

NOTE: When removing MM11-L memories, all three cards (G110, G231 and H214) must be removed. Verify and change, if necessary, address strapping of remaining MM11-L memories for contiguous address blocks starting from 0.

CONNECTOR COLUMNS

A	B	C	D	E	F	SLOT
MAINT	MAINT	**PERIPHERAL CONTROLLER				1
*UNIBUS TERMINATOR		DEC MEMORY STACK 1 H214				2
*** DEC MEMORY DRIVER 1 G231						3
*** DEC MEMORY CONTROL 1 G110						4
UNIBUS TERMINATOR		DEC MEMORY STACK 2 H214				5
*** DEC MEMORY DRIVER 2 G231						6
*** DEC MEMORY CONTROL 2 G110						7
PROCESSOR						8
PROCESSOR						9

COMPONENT SIDE
SOLDER SIDE

*OR EXTERNAL CABLE
**OR GRANT CONTINUITY CARD
***UNIBUS IS WIRED IN THESE SLOTS

DEC PDP-11/05 and PDP-11/10 Standard Module Utilization
Configuration 1 (16K)

CONNECTOR COLUMNS

A	B	C	D	E	F	SLOT
UNUSED		**PERIPHERAL CONTROLLER				1
MAINT	MAINT	**PERIPHERAL CONTROLLER				2
*UNIBUS TERMINATOR		**PERIPHERAL CONTROLLER				3
UNIBUS		**PERIPHERAL CONTROLLER				4
UNIBUS TERMINATOR		DEC MEMORY STACK H214				5
*** DEC MEMORY DRIVER G231						6
*** DEC MEMORY CONTROL G110						7
PROCESSOR						8
PROCESSOR						9

COMPONENT SIDE
SOLDER SIDE

*OR EXTERNAL CABLE
**OR GRANT CONTINUITY CARD
***UNIBUS IS WIRED IN THESE SLOTS

DEC PDP-11/05 and PDP-11/10 Standard Module Utilization
Configuration 2 (8K)

Figure 2

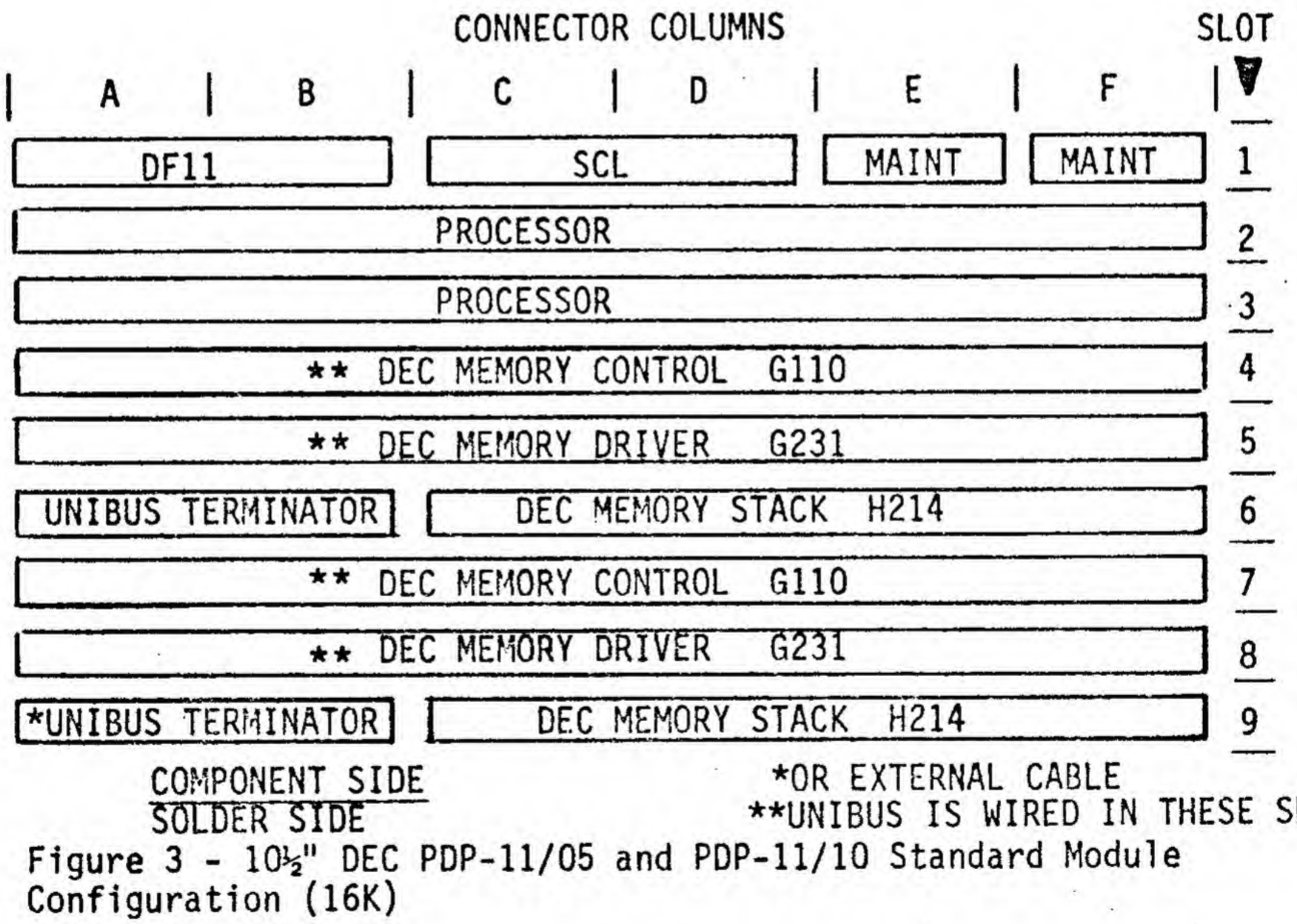


Figure 3 - 10½" DEC PDP-11/05 and PDP-11/10 Standard Module Configuration (16K)

2.2 Installation in Configuration 1 of 5¼" Assembly Unit

2.2.1 24K Word Configuration (Figure 4)

The 24K word configuration uses one DR-111 module and one MM11-L system.

The DR-111 is installed in slot 3. The stack blocks slot 4. The UNIBUS terminator remains in connectors 5A/5B. UNIBUS signals are available in slots 2A/2B and a UNIBUS terminator or external cable can be inserted in this location.

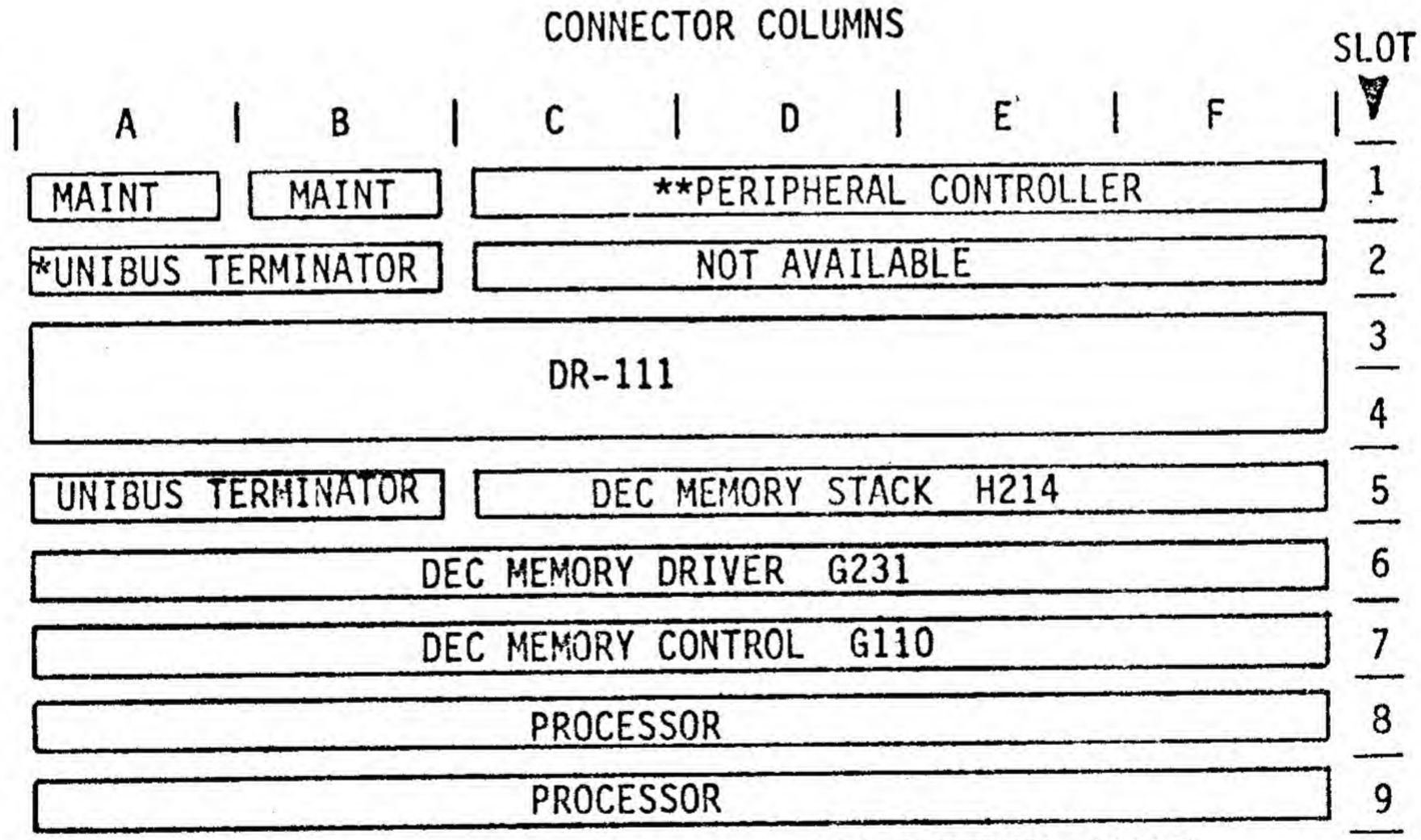


Figure 4 - 24K Word Installation Configuration 1 of PDP-11/05 and PDP-11/10

2.2.2 32K Word Configuration (Figure 5)

The 32K word configuration uses two DR-111 modules and no MM11-L.

The DR-111 modules are installed in slots 3 and 5. The stack board blocks the adjacent slots 4 and 6, respectively. The UNIBUS terminator board normally located in connectors 5A/5B is moved to connectors 7A/7B. The UNIBUS signals are also available in connectors 2A/2B. A UNIBUS terminator or cable can be inserted in this location.

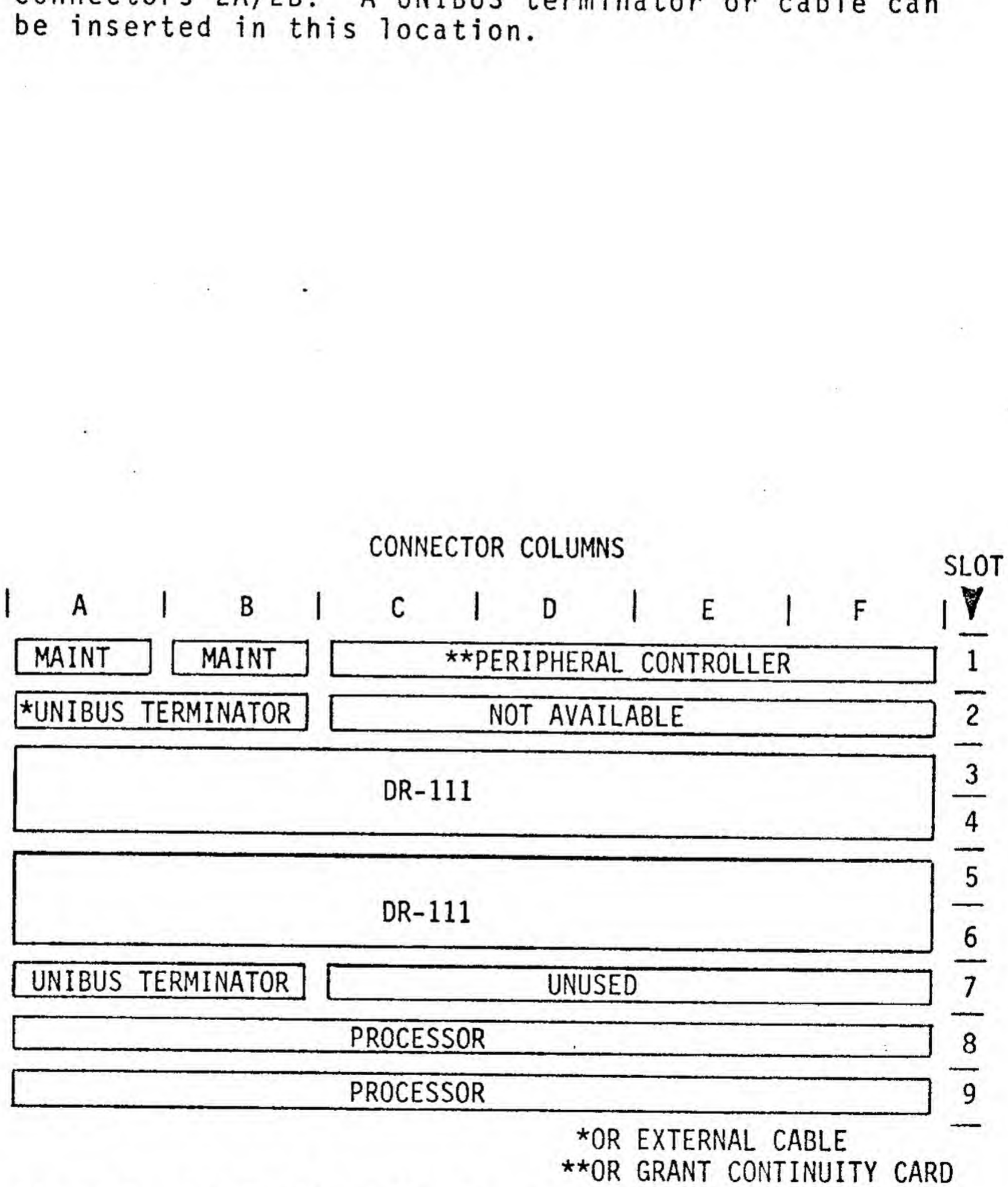


Figure 5 - 32K Word Installation Configuration 1 of PDP-11/05 and 11/10

2.3 Installation in Configuration 2 of 5¼" Assembly Unit

2.3.1 16K Word Configuration (Figure 6)

The 16K word configuration has one DR-111 module, four peripheral controllers and no MM11-L.

The DR-111 is installed in slot 5. Slot 6 is blocked by the stack board. The UNIBUS terminator normally located in connectors 5A/5B is moved to connectors 7A/7B. Connectors 3A/3B and 4A/4B are available for installation of either a second terminator or UNIBUS cable.

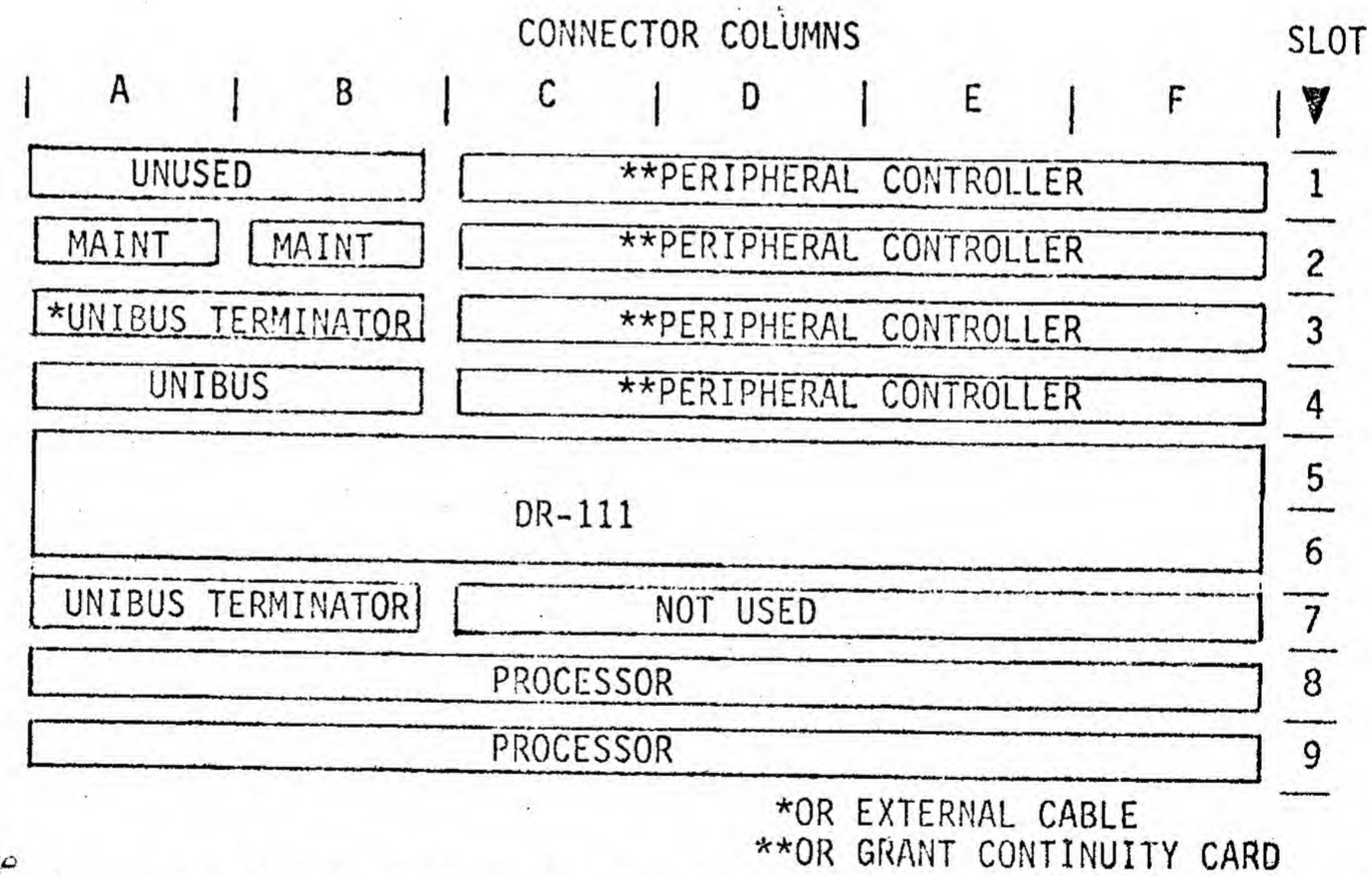


Figure 6 - 16K Word Installation in Configuration 2 of PDP-11/05 and PDP-11/10

2.3.2 24K Word Configuration (Figure 7)

The 24K word configuration has one DR-111 module, one MM11-L and two peripheral controllers.

The DR-111 module is installed in slot 3. Although the stack partially blocks slot 4, there is sufficient room available to plug a UNIBUS cable in connectors 4A/4B and a Grant Continuity Card in connector 4D. If it is necessary to terminate the UNIBUS in connectors 4A/4B, a special terminator board, DRC part number 61106, may be purchased from Dataram for installation in this location. The standard DEC M930 terminator will not fit mechanically in this application.

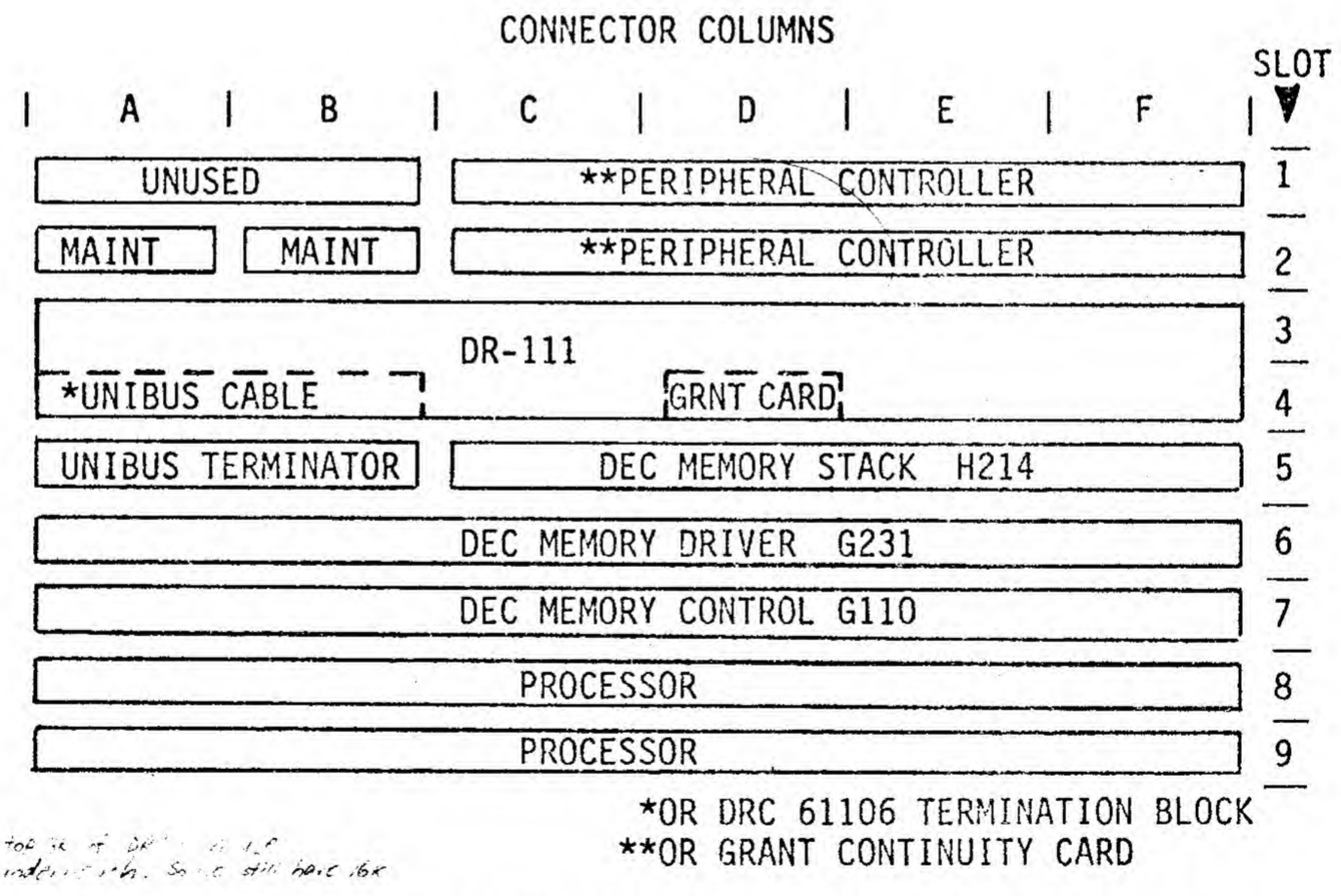


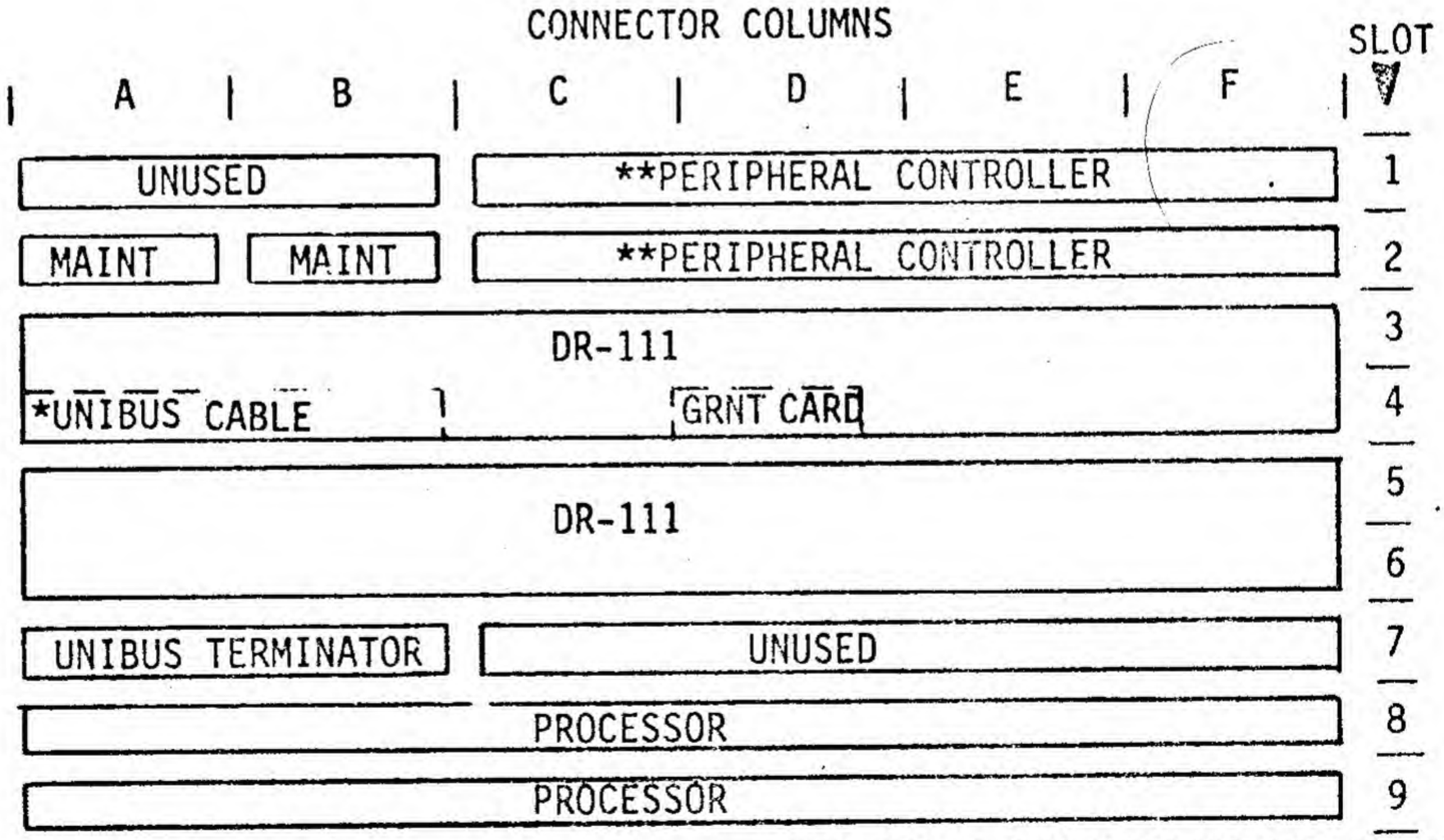
Figure 7 - 24K Word Installation Configuration 2 of PDP-11/05 and PDP-11/10

2.3.3 32K Word Configuration (Figure 8)

The 32K word configuration has two DR-111 modules and two peripheral controllers.

The DR-111 modules are installed in slots 3 and 5. The stack partially blocks slots 4 and 6.

The UNIBUS terminator normally located in connectors 5A/5B is moved to connectors 7A/7B. Although the stack partially blocks slot 4, there is sufficient room available to plug a UNIBUS cable in connectors 4A/4B and a Grant Continuity Card in connector 4D. If it is necessary to terminate the UNIBUS in connector 4A/4B, a special terminator board, Dataram part number 61106, may be purchased from Dataram for installation in this location.



*OR DRC 61106 TERMINATION BLOCK
**OR GRANT CONTINUITY CARD

Figure 8 - 32K Word Installation Configuration 2 of PDP-11/05 and PDP-11/10

2.4 Installation in 10½" Assembly Unit

2.4.1 24K Word Configuration (Figure 9)

The 24K word configuration uses one DR-111 module and one MM11-L system.

The DR-111 is installed in slot 4. The stack blocks slot 5. The UNIBUS terminator remains in connectors 6A/6B. UNIBUS signals are available in slots 9A/9B and a UNIBUS terminator or external cable can be inserted in this location.

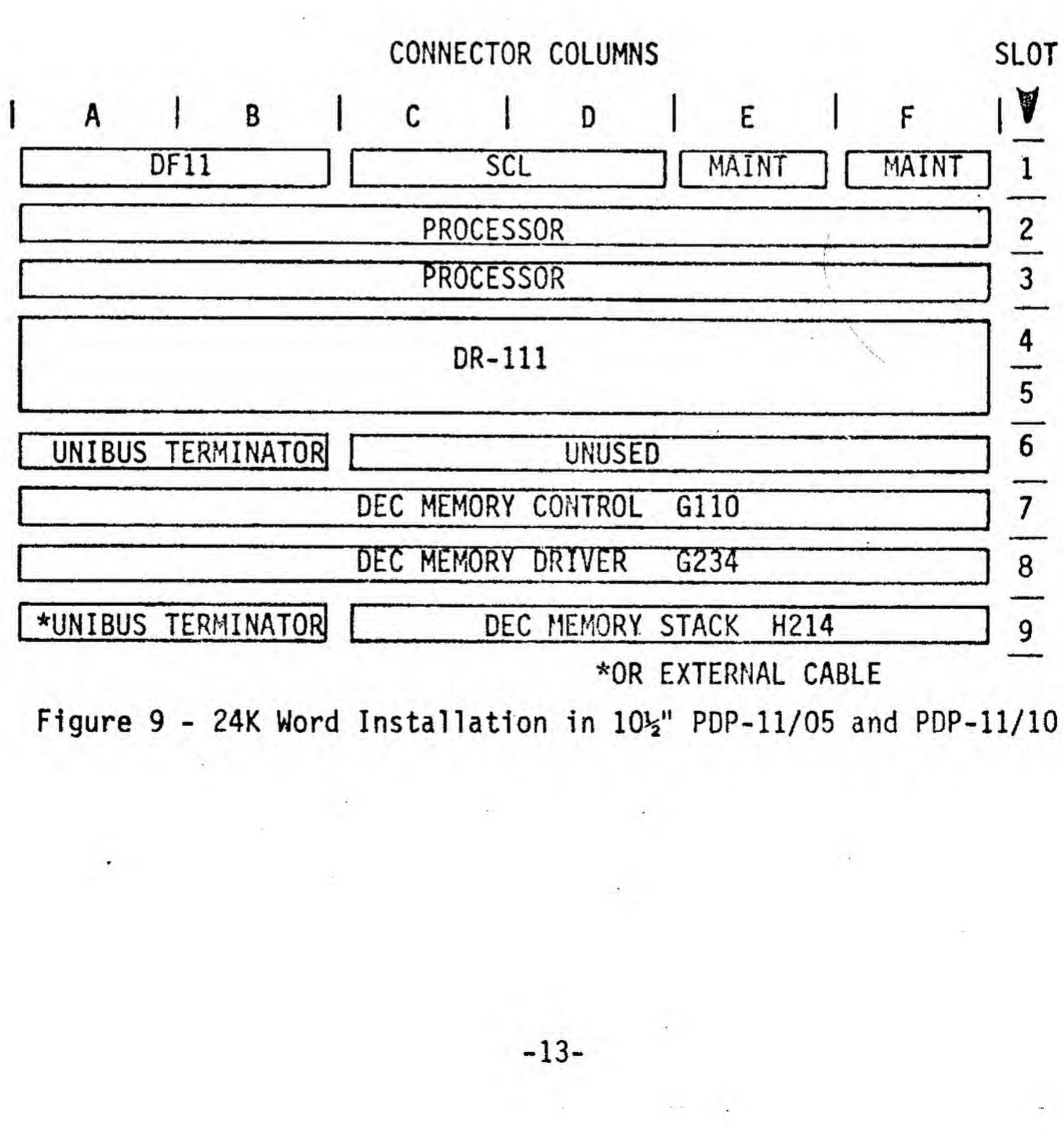


Figure 9 - 24K Word Installation in 10½" PDP-11/05 and PDP-11/10

2.4.2 32K Word Configuration (Figure 10)

The 32K word configuration uses two DR-111 modules and no MM11-L.

The DR-111 modules are installed in slots 4 and 7. The stack board blocks the adjacent slots 5 and 8, respectively. The UNIBUS terminator board is located in connectors 6A/6B. The UNIBUS signals are also available in connectors 9A/9B. A UNIBUS terminator or cable can be inserted in this location.

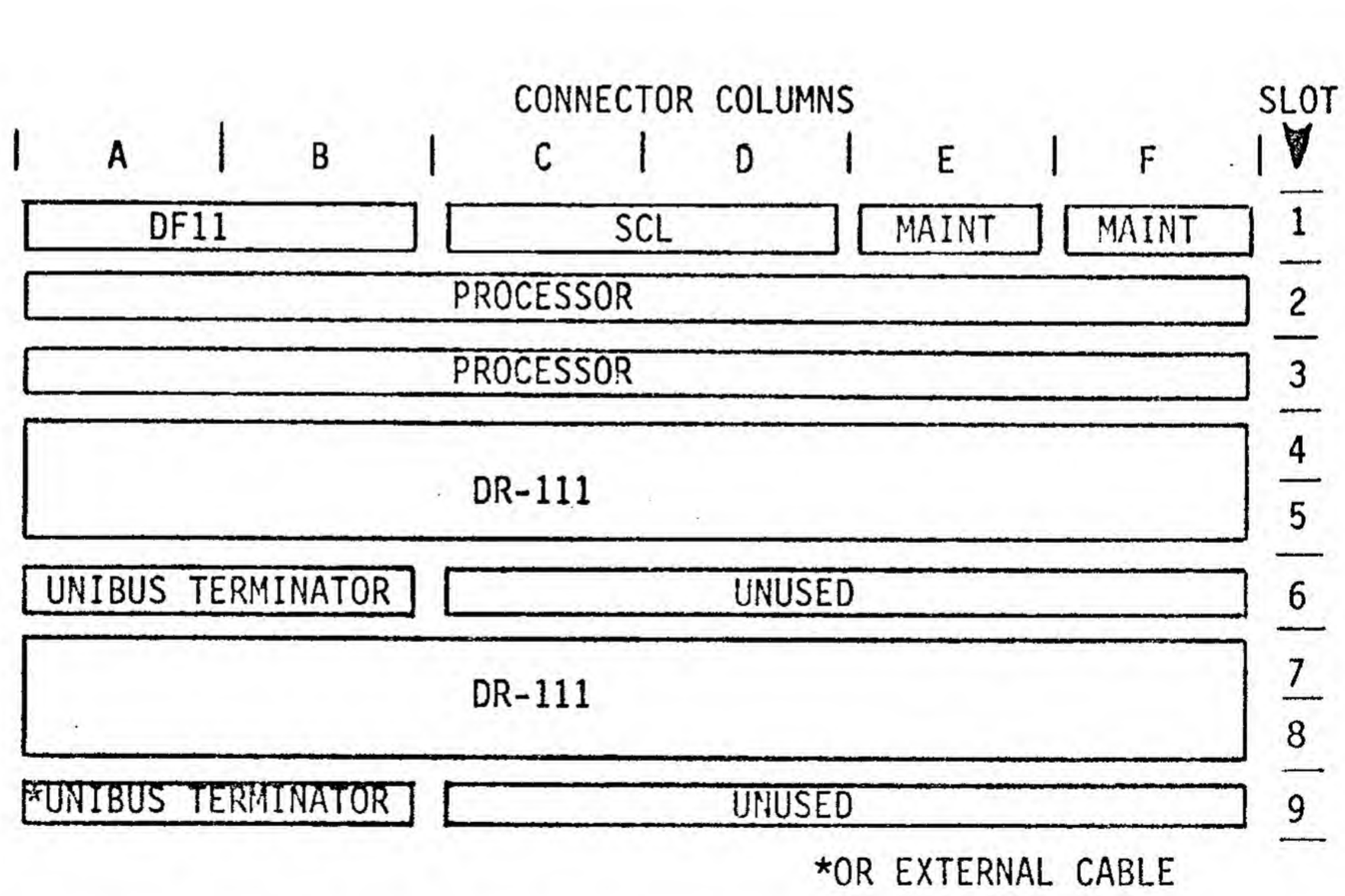


Figure 10 - 32K Word Installation in 10½" PDP-11/05 and PDP-11/10

3.0 INSTALLATION IN THE MF11-L ASSEMBLY UNIT OF THE PDP-11/35, PDP-11/40, PDP-11/45 COMPUTERS AND ME11-L EXPANSION CHASSIS

3.1 Standard DEC Configurations

The basic PDP-11/35, 40 and 45 computers consist of two double system units, each unit containing nine rows of connectors. The first nine slot system unit contains the processor and associated option boards and is not used for memory installation. The second nine slot system unit is prewired for DEC memory modules. In many installations, this double system unit is an MF11-L assembly unit which generally contains 8K to 24K of MM11-L memory. There is room in each computer for additional MF11-L system units for memory expansion. Some installations may contain other memory assembly units which are discussed in Section 5.

The ME11-L is a completely self-contained system. It is an MF11-L mounted in a 5¼" high box that includes a power supply. The ME11-L is used for memory expansion for all PDP-11 computers, such as, the PDP-11/05, PDP-11/10, PDP-11/15, PDP-11/20, PDP-11/35, PDP-11/40 and PDP-11/45.

This section describes typical installation details for mounting DR-111 modules in the MF11-L assembly with or without MM11-L memories. Memory expansion beyond the basic unit is identical when other MF11-L backplanes are installed. Figure 11 shows slot allocation for a fully expanded 24K MF11-L assembly using MM11-L memories. Connectors 1A/1B and 9A/9B are used either to extend or to terminate the UNIBUS. The standard UNIBUS jumper is used to extend the bus from system unit to system unit. The terminator is installed in the last system unit at or near the end of the bus. Using these requirements, the following subsections describe various word capacities using DR-111 modules.

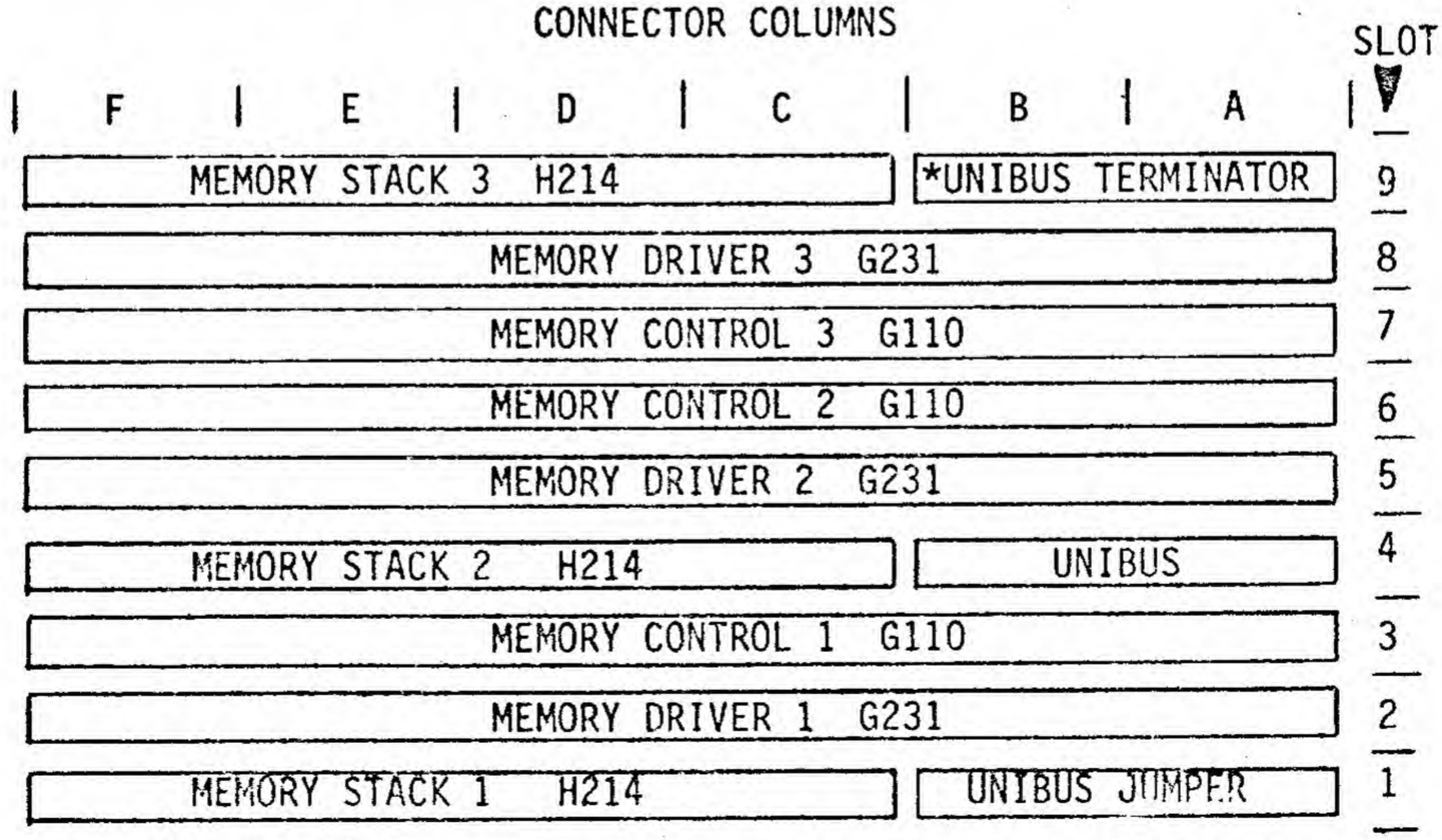


Figure 11 - Standard DEC MF11-L Memory Configuration

3.2 16K, 32K, 48K and 64K Word Configurations (Figure 13)

These configurations use up to three DR-111 modules. Memory Management is required for the 48K word and 64K word configurations. For 48K words, the DR-111 modules are installed in slots 2, 4 and 6.

A 32K word capacity can be configured by installing two DR-111 modules in slots 2 and 4. Similarly, 16K words can be configured by installing one DR-111 module in slot 2.

The 64K word capacity can be configured by installing another DR-111 module in slot 8. Although the stack partially blocks slot 9, the UNIBUS cable or jumper will fit in connector 9A/9B. If it is necessary to terminate the UNIBUS in connector 9A/9B, a special terminator, DRC part number 61106, may be purchased from Dataram for installation in this location.

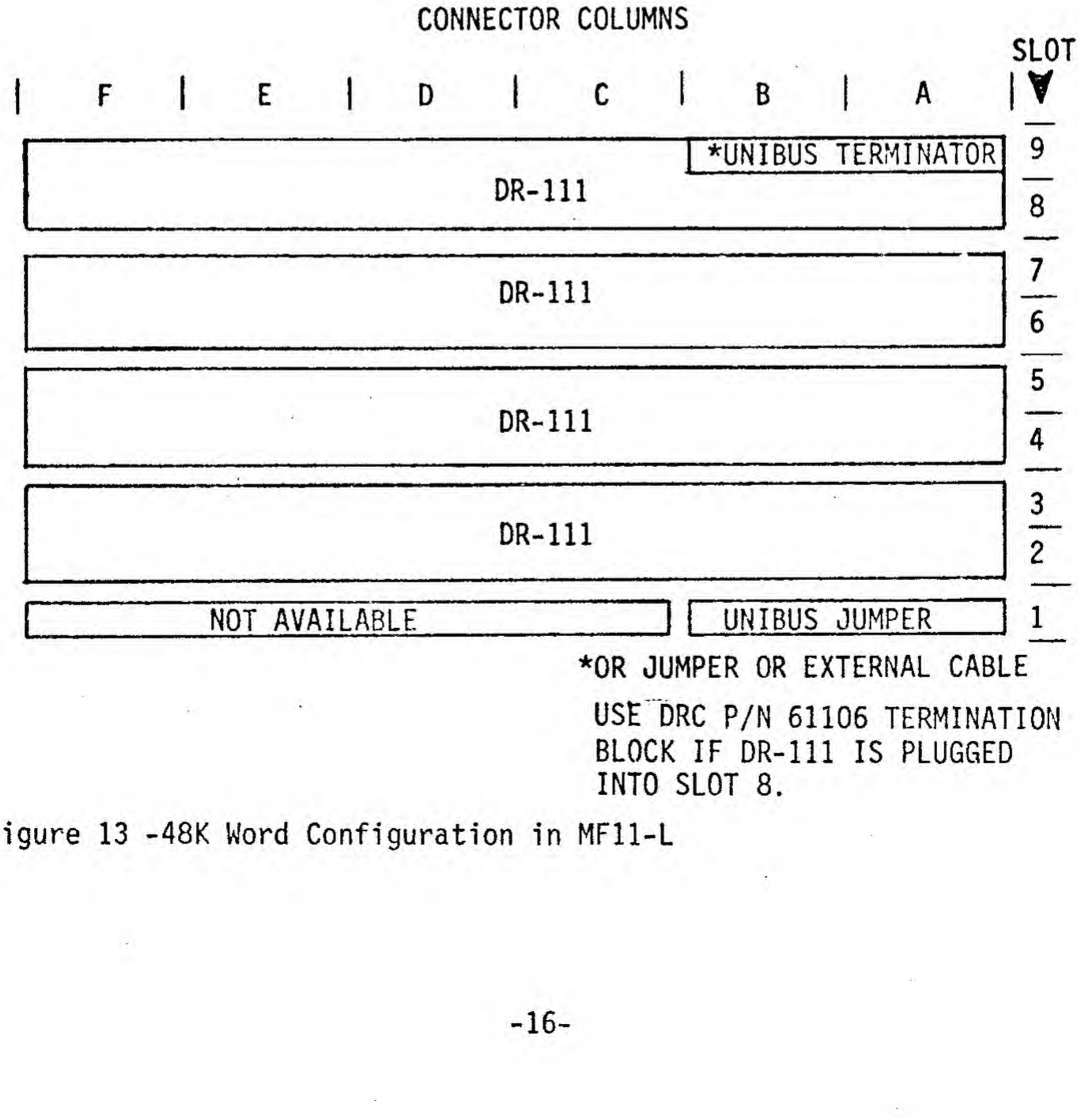


Figure 13 -48K Word Configuration in MF11-L

3.3 24K Word and 40K Word Configurations (Figure 12)

These configurations use one MM11-L memory and up to two DR-111 modules. Memory Management is required for the 40K word configuration. The DR-111 modules are installed in slots 5 and 7.

A 24K word capacity can be configured by installing only one DR-111 module in slot 5.

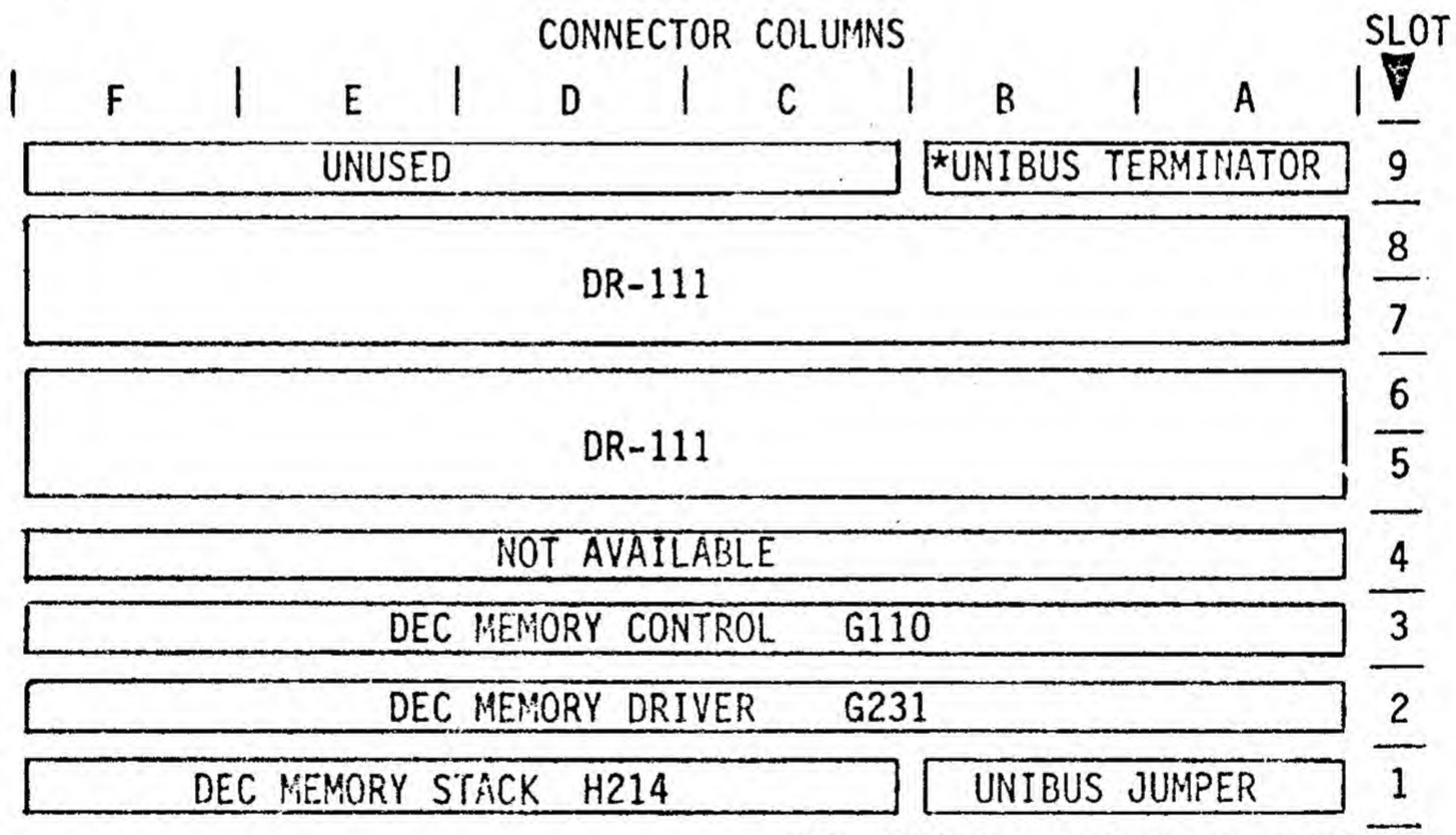


Figure 12 - 40K Word Installation in MF11-L

3.4 32K Word Configuration (Figure 14)

This configuration uses two MM11-L memories and one DR-111 module.

The DR-111 module is installed in slot 7.

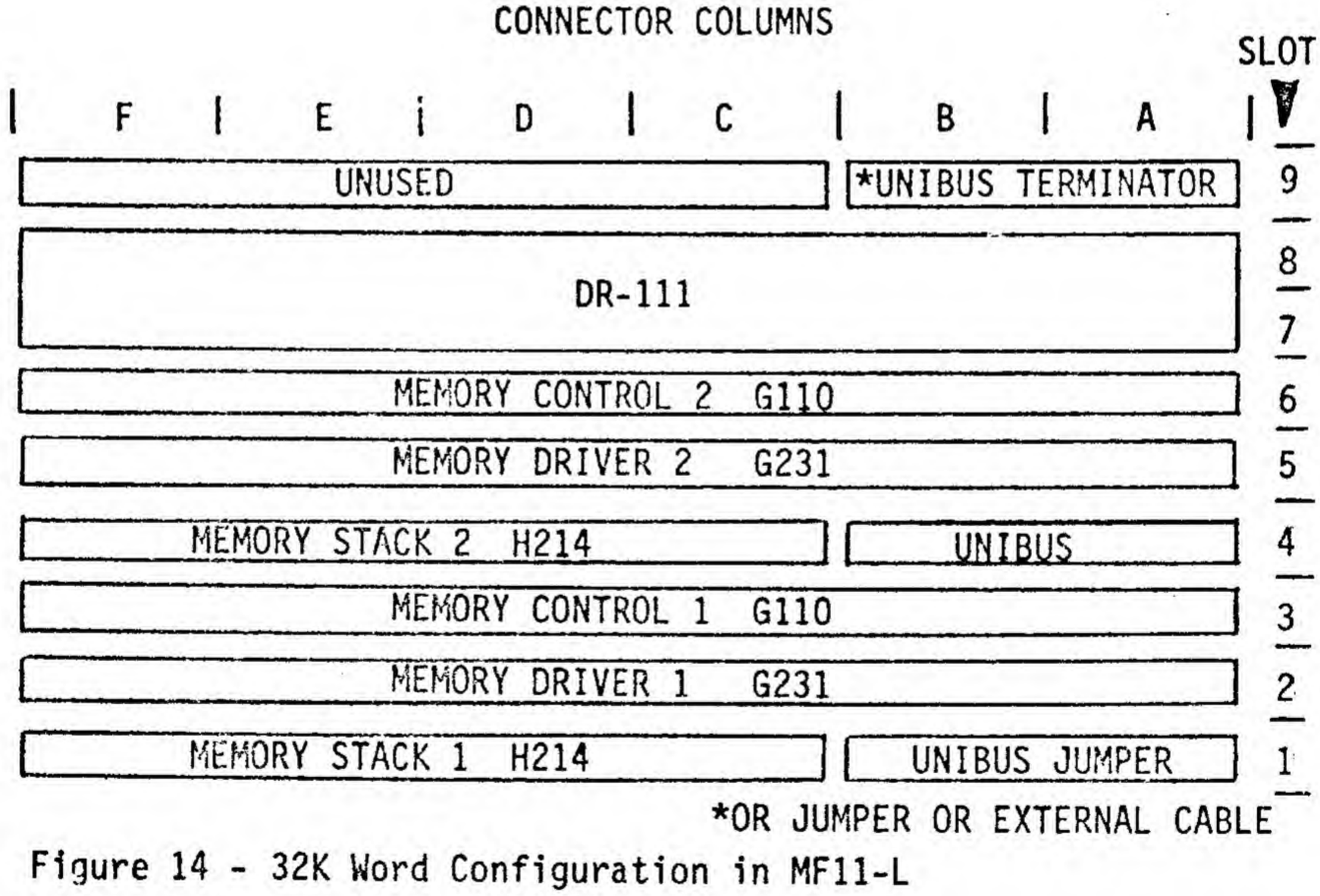


Figure 14 - 32K Word Configuration in MF11-L

4.0 INSTALLATION IN THE PDP-11/15 AND PDP-11/20 COMPUTERS

Although the DR-111 is electrically compatible with the PDP-11/15 and PDP-11/20 UNIBUS signals, it cannot physically fit inside the BA11-CC or BA11-CS mounting boxes.

However, there are application where the basic machine is expanded with an ME11-L extension box. DR-111 modules can be installed in this equipment as described in section 3.0.

5.0 SPECIAL DEC CONFIGURATIONS

5.1 MF11-LP Assembly Unit and ME11-LP Extension Box

The MF11-LP and ME11-LP are wired for the MM11-LP memories. These memories (8K x 18) contain two extra bits for parity signals. The DR-111 modules are 16K x 16 systems and cannot be used for these applications. If the DR-111 module is inserted accidentally into the MF11-LP or ME11-LP, the DR-111 or CPU will not be damaged.

5.2 MF11-U, MF11-UB, MF11-UC, MF11-UP, MF11-UR and MF11-US Assembly Units

The MF11-U series assembly units are double system units wired to accept two DEC MM11U or MM11-UP 16K x 16 memory systems. The MM11-U and MM11-UP memory modules are designed to operate from different supply voltages than the MM11-L modules. The backplane wiring of the MF11-U series assembly units is such that these voltages appear at connector pins used by the DR-111 modules. If a DR-111 module is installed in the MM11-U series assembly units, COMPONENTS ON THE DR-111 WILL BE DAMAGED!

The drawing in Figure 15 shows the configuration of the MF11-U series assembly units.

For identification purposes, the following is a list of the modules used to configure an MM11-U memory:

M8293	Timing and Control Module
G114	Sense and Inhibit Module
G235	X/Y Driver Module
H217D	Memory Stack Module
H217C	Memory Stack Module (MM11-UP)
M7259	Parity Module (MM11-UP)

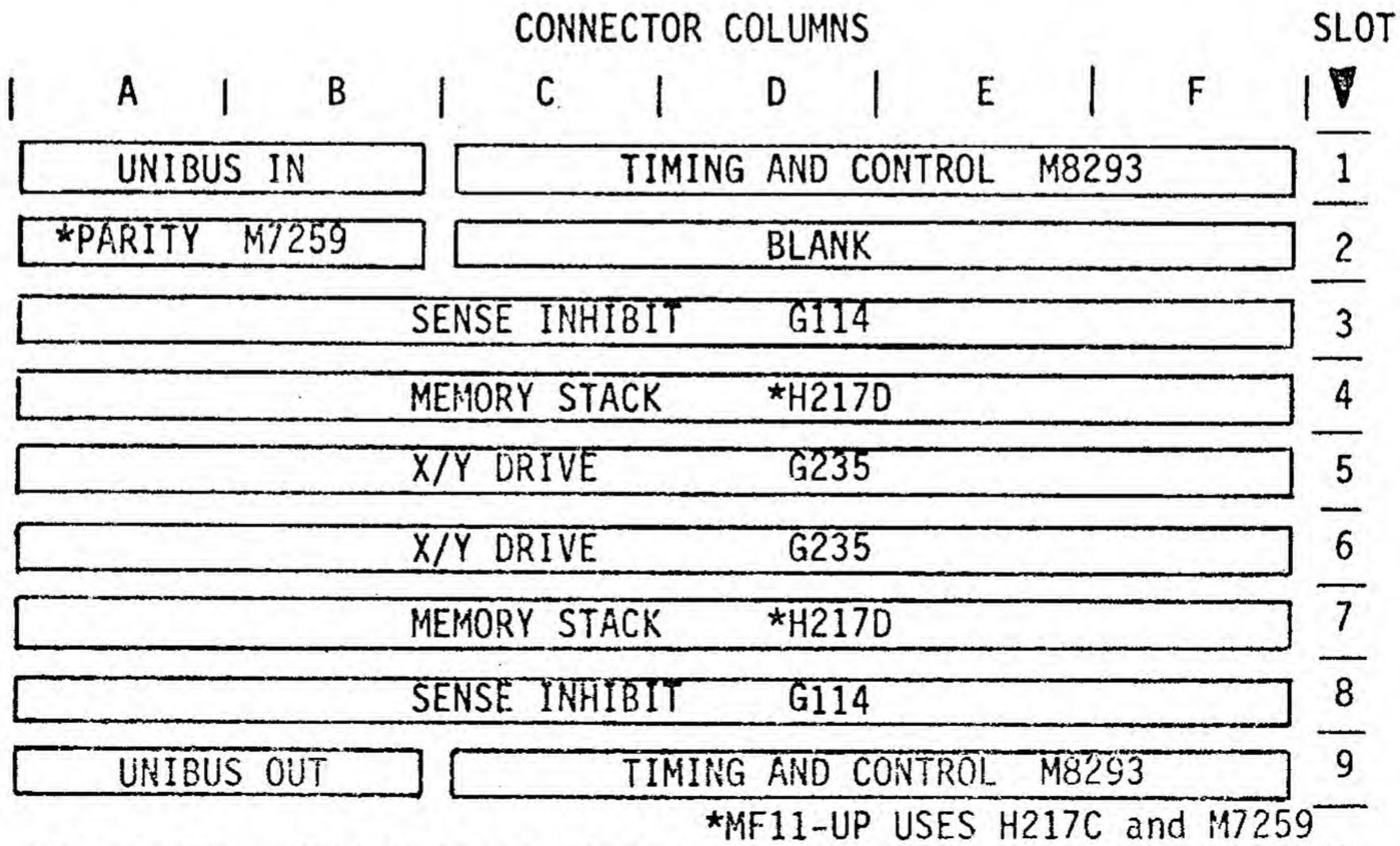


Figure 15 - MF11-U Series Standard DEC Module Utilization (32K)

COMPONENT SIDE
SOLDER SIDE

CORE MEMORY SYSTEM

DR-111

TABLE OF CONTENTS

1.0 DESCRIPTION

1.1 General

The Dataram Corporation Model DR-111 memory system is designed to operate in Digital Equipment Corporation's PDP-11 computers. The DR-111 memory may be operated with, or in place of, the DEC Model MM11-L or the MM11-K memories.

The DR-111 can be installed directly into various models of the PDP-11 series computers and expansion units. They include:

A. PDP-11/05 and PDP-11/10

B. PDP-11/15 and PDP-11/20

C. PDP-11/35 and PDP-11/40

D. PDP-11/45

E. ME11-L and MF11-L

2.0 SYSTEM SPECIFICATIONS

2.1 System Characteristics

2.1.1 Capacity

The storage capacity of the basic DR-111 memory is 16,384 words by 16 bits. The system is also available with 8,192 words by 16 bits.

A maximum capacity of 128K words by 16 bits is available by combining 8 memory assemblies. Memory extension is available as a Unibus expansion option and allows a total of 124K by 16 bit words of memory to be used in the computer. The upper 4K of 128K is reserved for I/O device addresses.

2.1.2 Modes

DATI	Read/Restore
DATIP	Half Cycle Read
DATO	Clear/Write
DATOB 0	Read/Restore Byte 1 Clear/Write Byte 0
DATOB 1	Read/Restore Byte 0 Clear/Write Byte 1

2.1.3 Cycle Time

900 nanoseconds	DATI, DATO or DATOB
600 nanoseconds	DATIP (and DATO following DATIP)

2.1.4 Access Time

The access time of the DR-111 memory is 350 nanosec or less. The access time is measured at the Unibus connector of the memory module. The time delay between the +1.5 volt levels of the MSYN pulse and SSYN during memory read cycles is defined as "access time". See Figure 3.

2.1.5 Power Requirements

The DR-111 memory system requires the same DC voltages as the DEC memory. The voltage-current requirements are as follows for each 16,384 by 16 memory assembly:

	Operating Amps	Standby Amps	Voltage Tolerance
+5V	3.5	2.0	±5%
-15V	4.5	0.2	±5%

2.2 Addressing

The DR-111 memory will accept a full 18 bit address with the least significant bit being used for byte selection. The address lines to the memory are single rail; the addressing mode may be random. The address lines are identified as A0 through A17.

A0 is used for byte selection. A1 through A14 are decoded for 1 of 16,384 address locations within any memory module.

A13 through A17 are "strappable" on the memory module. These address lines may be strapped to set the initial address for a memory module. A 16 pin dual-in-line socket is provided to accommodate the strapping jumpers. The initial address may be any of the following:

Initial Address	Pin 2	Pin 7	Pin 4		Jumper		
			8K	16K	R	W	
0	3	8	16,15	16-13	P	V	
4K	3	8	15,14	15-12	P	V	
8K	3	8	14,13	14-11	P	V	
12K	3	8	13,12	13-10	P	V	
16K	3	8	12,11	12-9*	P	V	
20K	3	8	11,10	11-9 & 5	U	V	
24K	3	N/C	10,9*	15 & 10	P	U	
32K	3	6	16,15	16-13	P	V	
40K	3	6	14,13	14-11	P	V	
48K	3	6	12,11	12-9	P	V	
56K	3	N/C	10,9	9 & 5	P	U	
64K	1	8	16,15	16-13	P	V	
72K	1	8	14,13	14-11	P	V	
80K	1	8	12,11	12-9	P	V	
88K	1	N/C	10,9	15 & 10	P	U	
96K	1	6	16,15	16-13	P	V	
104K	1	6	14,13	14-11	P	V	
112K	1	6	12,11	12-10	P	V	(124K Max.)
120K	1	N/C	10	N/A	P	U	

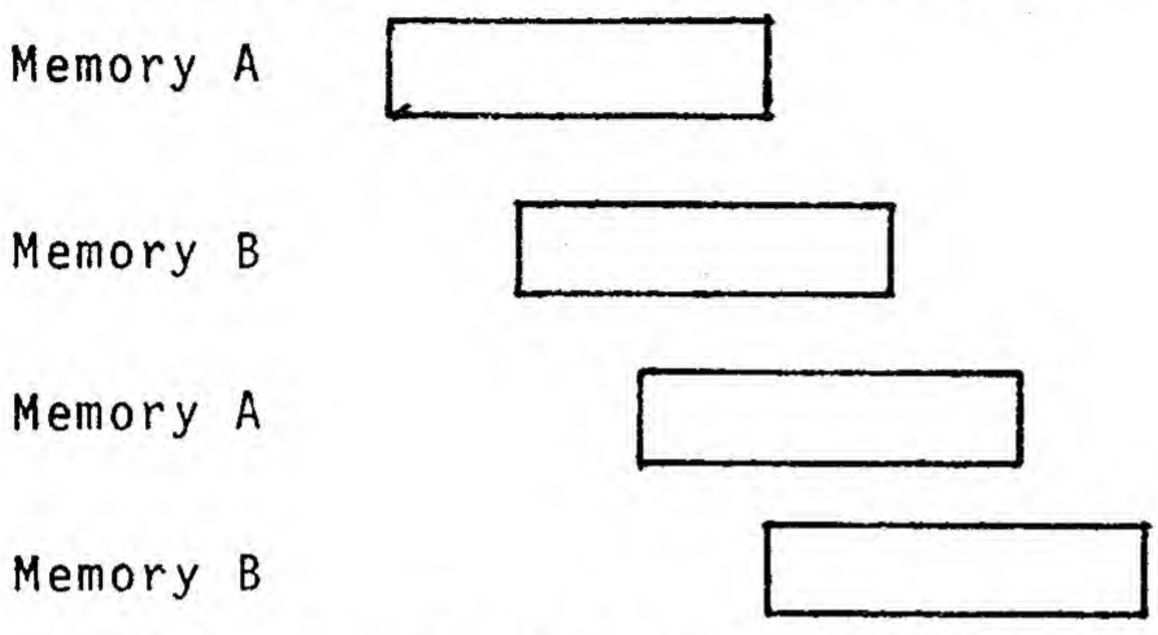
* Jumper T-S for 31K operation.

JUMPER LOCATIONS FOR MEMORY STRAPPING

TABLE I

2.2.1 Interleaving

Two DR-111 memories may be interleaved to provide a faster cycle time when used in the PDP-11 processor. When two memory modules have been interleaved, odd numbered addresses are assigned to memory module A and even numbered addresses are assigned to memory module B. During normal processing, the loading and unloading of core memory is accomplished in a sequential manner. The DR-111 has its own address and data registers, therefore, it is possible for the CPU to start memory A and, before memory A has completed its cycle, the CPU may start memory B.



The DR-111, if used as an 8K module, may be interleaved with another 8K memory module such as the DEC MM11-L.

The two sections of one DR-111 may not be interleaved.

Pin	Signal
CA2, DA2	+5 V
EA2, FA2	+5 V
CB2, DB2	-15 V
EB2, FB2	-15 V
CC2, DC2	OV
EC2, FC2	OV
CT1, DT1	OV
ET1, FT1	OV

DK2	BUS GRANT	1 IN
DL2	BUS GRANT	1 OUT
DM2	BUS GRANT	2 IN
DN2	BUS GRANT	2 OUT
DP2	BUS GRANT	3 IN
DR2	BUS GRANT	3 OUT
DS2	BUS GRANT	4 IN
DT2	BUS GRANT	4 OUT

All other pins not listed above are open circuit.

TABLE III

2.3 Interface

The memory interfaces with the processor or other memories or peripherals via the Unibus. The Unibus signals and their appropriate pin numbers are shown in Table IV. The memory also provides jumpers for passing the bus grant lines through the memory. See Table III for pin connections.

Signal	DEC No.		Signal
INIT L	AA1	AA2	+5 V 2
1 INTR L	AB1	AB2	OV
D00 L	AC1	AC2	OV
D02 L	AD1	AD2	D01 L
D04 L	AE1	AE2	D03 L
D06 L	AF1	AF2	D05 L
D08 L	AH1	AH2	D07 L
D10 L	AJ1	AJ2	D09 L
D12 L	AK1	AK2	D11 L
D14 L	AL1	AL2	D13 L
1 PA L	AM1	AM2	D15 L
OV	AN1	AN2	PB L 1
OV	AP1	AP2	BBSY L 1
OV	AR1	AR2	SACK L 1
OV	AS1	AS2	NPR L 1
OV	AT1	AT2	BR7 L 1
1 NPG H	AU1	AU2	BR6 L 1
1 BG7 H	AV1	AV2	OV
1 BG6 H	BA1	BA2	+5 V 2
1 BG5 H	BB1	BB2	OV
1 BR5 L	BC1	BC2	OV
OV	BD1	BD2	BR4 L 1
OV	BE1	BE2	BG4 L 1
1 ACLO L	BF1	BF2	DC LOL
A01 L	BH1	BH2	A00 L
A03 L	BJ1	BJ2	A02 L
A05 L	BK1	BK2	A04 L
A07 L	BL1	BL2	A06 L
A09 L	BM1	BM2	A08 L
A11 L	BN1	BN2	A10 L
A13 L	BP1	BP2	A12 L
A15 L	BR1	BR2	A14 L
A17 L	BS1	BS2	A16 L
OV	BT1	BT2	C1 L
SSYN L	BU1	BU2	C0 L
MSYN L	BV1	BV2	OV

Note 1 Pins assigned in Unibus connector, but not used in memory.

2 +5 V used for termination only.

UNIBUS SIGNALS

TABLE IV

2.3.1 Input Signals

Signals required by the memory are listed below:

A0-A17	ADDRESS LINES
C0, C1	CONTROL LINES
MSYN	MASTER SYNC
INIT	INITIALIZE
DC OK	DC POWER OK
D0-D15	DATA LINES

All signals terminate at the memory in National DM8837N or DM8838N unified bus receiver/transceiver integrated circuits.

2.3.2 Output Signals

Output signals for the memory are listed as follows:

D0-D15	DATA LINES
SSYN	SLAVE SYNC

The D0-D15 output signals from the memory are driven by National DM8838N quad unified bus transceivers.

2.3.3 System Installation

For system location and installation refer to Dataram Installation Manual 06011.

2.4 Mechanical

The DR-111 memory system is designed to fit mechanically into the PDP-11 computer utilizing the space of two DEC Standard Hex printed circuit boards. Section 4.1 of Documentation shows the location of the DR-111 system in various modes.

Each memory module has a storage capacity of 16,384 words by 16 bits. The magnetics assembly plugs onto the rear of the memory electronics board using Amp Mod I connectors. The dimensions of the memory module are .78 x 8.96 x 15.58 inches and it occupies two card slots in the computer chassis.

2.5 Environmental

The DR-111 memory is capable of sustained operation in the PDP-11 computer over the temperature range of 0°C to +50°C and 0 to 90% relative humidity.

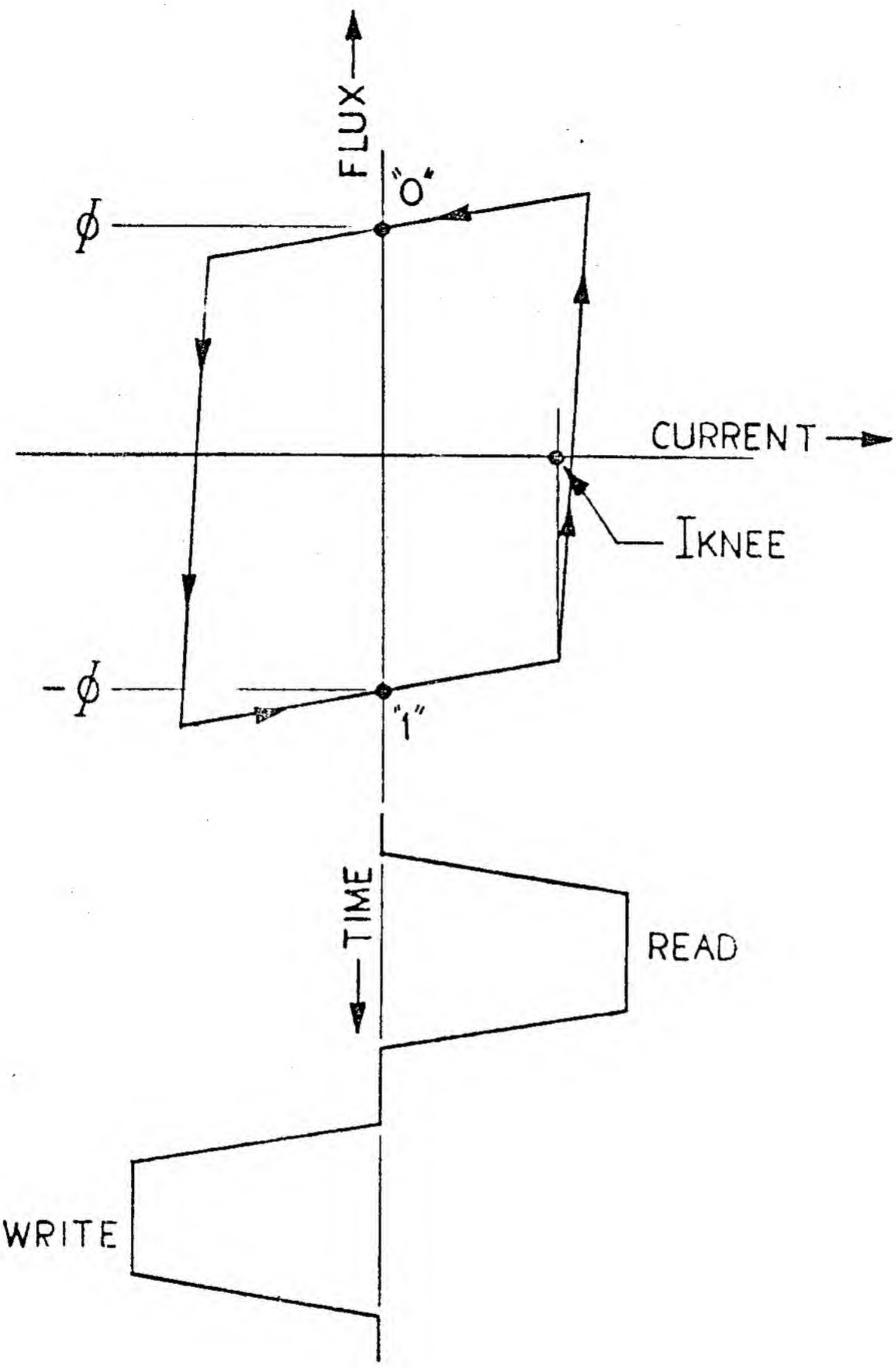
3.0 THEORY OF OPERATION

3.1 3D-3 Wire Organization

A coincident-current core memory, such as the DR-111, has as its basic storage element, a ferrite core, which has a well-defined switching characteristic. Its operation will be explained by referring to Figure 1. This figure defines the switching characteristic of the core and is known as the "hysteresis loop". It shows the relationship of the flux (magnetic field strength) in the core with respect to the total current flowing through the core aperture. Flux above the origin can be arbitrarily defined as flux in the clockwise direction and flux below the origin will be counterclockwise. The direction of flux will define the storage of a "1" or a "0". Currents on either side of the origin will have opposite directions of current flow through the core. In this explanation, current to the right of the origin will be considered "Read" current and to the left will be "Write" current. A core can be in a "1" or "0" state as shown on the hysteresis loop.

If it is in the "1" state, a Read current will put it in the "0" state and the flux will change from $-\Phi$ to $+\Phi$ which means the flux will flip from a counterclockwise orientation to clockwise. This change in flux (2Φ) will cause a voltage to be induced on the sense wire which threads the core being interrogated by the Read current and this voltage will be detected as a "1" by the sensing circuitry connected to the sense wire. In the DR-111 system, the "1" output is approximately 30 millivolts. If the core had been in the "0" state, Read current would cause only a relatively small (approximately 4 millivolts in DR-111) change in flux and, therefore, the induced voltage would be seen as a "0" by the sensing circuitry since it is below the minimum detection level.

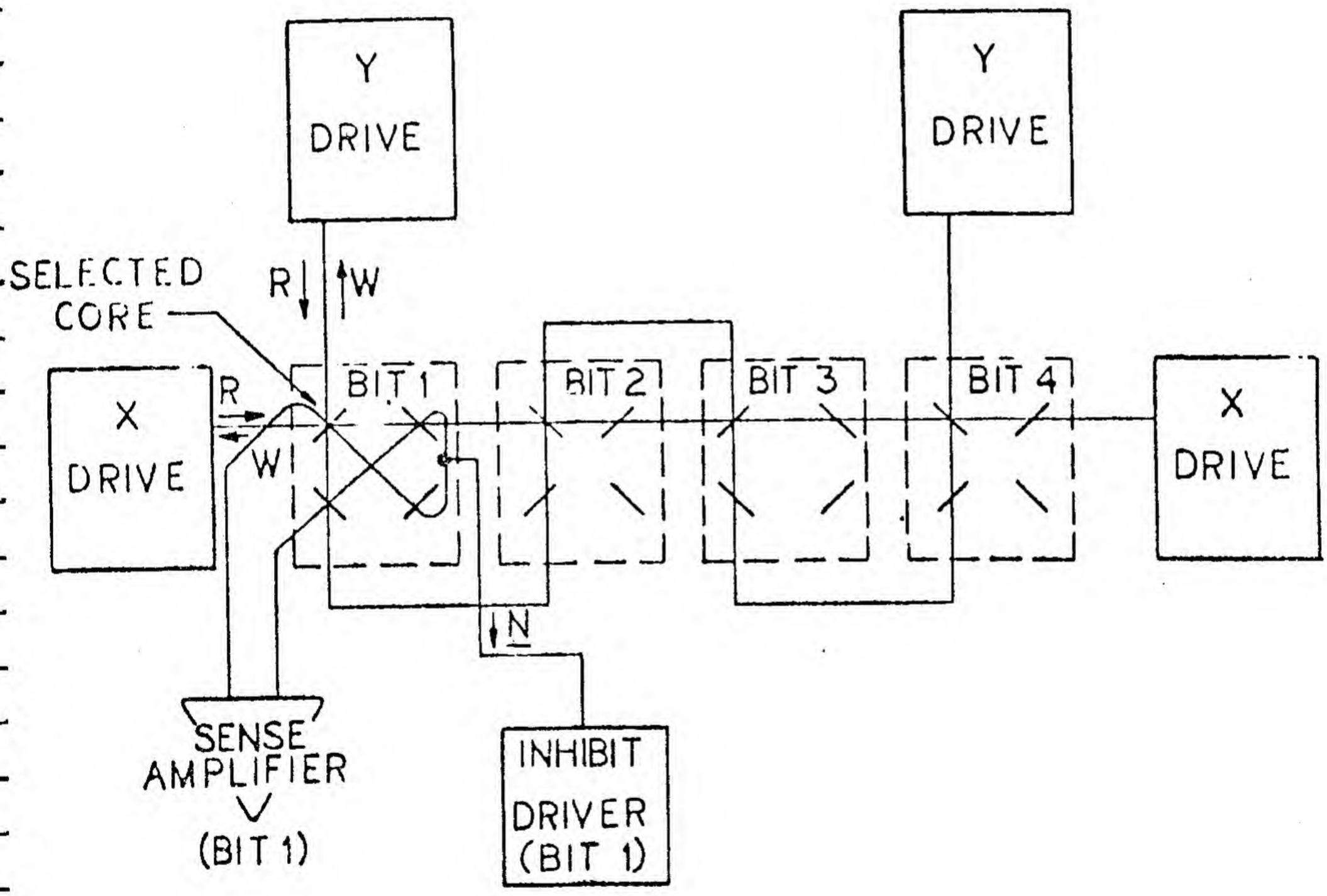
To Write, the switching current polarity will be opposite in polarity in relation to the Read current. The Write current will cause the flux to go to a counterclockwise orientation which defines the core as being in the "1" state. When the core does not receive a full Write current during a Write operation, it will stay in the "0" state.



HYSTERESIS LOOP

FIGURE 1

Selection of a particular word in a memory array is shown in Figure 2. The intersection of selected X and Y drive lines in an array will cause the same corresponding core in each bit plane to be pulsed by full Read and full Write currents. In Figure 2, the top left core of each bit plane is selected and the number of bit planes define the number of bits per word. Some unselected cores may experience half-amplitude currents, but the amplitude of these half-amplitude currents will not be sufficient to exceed the knee on the hysteresis loop (see Figure 1) and the core will remain in its previous state.



3D-3 WIRE SCHEME

FIGURE 2

The coincidence of half-Write currents at the selected core location in each bit would cause the selected core to experience full Read and Write currents. This is desired during a Read operation but during a Write operation, it is necessary to control the Write current so that either a "1" or a "0" may be written. This is accomplished by using the sense winding as an inhibit winding during Write time and an inhibit driver per bit array. The sense/inhibit winding threads every core in the bit array and the inhibit driver will pulse current through this winding when a "0" is to be written. The inhibit current has the opposite polarity to write current and when it is "on" it cancels one of the two half write currents. The resultant current will be a half-Write, which will be insufficient to switch the core and it will remain in the "0" state.

3.2 System Description

The DR-111 memory system may be broadly divided into four basic subdivisions.

a. Timing and Control Circuitry

b. Planar Core Array

c. X & Y Current Drive Circuitry

d. Data Loop Circuitry

3.2.1 Timing and Control Circuitry

The memory, which can only act as a slave to the processor or I/O device, receives commands, address and data information on the Unibus. The internal circuitry of the memory responds to these signals in the following sequence:

a. The address information on the Unibus is examined.

b. If the address does not fall within the address block to which the memory is strapped, it continues to remain in its non-cycling state. Otherwise, the mode formation on the Unibus is decoded. Timing signals necessary to perform the required mode are generated simultaneously and address bits 1 through 14, control signals C1 and C2 are stored. If the required mode happens to be a Write operation, then the data bits are also stored at the same time. (See Figures 3 and 4)

3.2.1.1 Modes of Operation

The operating mode of the memory is determined by the state of the C0 and C1 control lines and the A0 address lines. These modes are defined as follows:

A0	C1	C0	Command	Operation
X	0	0	DATI	Read/Restore
X	0	1	DATIP	Half Cycle Read
X	1	0	DATO	Clear/Write
0	1	1	DATOB 0	Read/Restore Byte 1 Clear/Write Byte 0
1	1	1	DATOB 1	Read/Restore Byte 0 Clear/Write Byte 1

The control lines may be sequenced in any manner, however, the operation immediately following a DATIP will be forced by the memory logic to be half cycle write. The processor will normally send a DATO or DATOB after a DATIP and these commands will be converted by the memory logic to half cycle write operations.

3.2.1.1.1 Data-In, DATI or DATIP

Data-In is the data transfer from the DR-111 memory to a master. DATI and DATIP are similar data-in operations.

Figure 3 shows the timing between master and memory for a typical DATI or DATIP. A bus master places the address and required control bits on the A and C Unibus lines. The memory decodes these A and C signals to see if it is selected as the slave for this transfer.

The master waits after putting the address and control bits on the A and C lines. If the previous slave has ended its part of the preceding data cycle by negating SSYN, the master asserts MSYN.

The selected memory, after receiving the assertion of MSYN, places the requested data on the D lines and asserts SSYN.

The master receives the assertion of SSYN, strobes the data and negates MSYN.

The receipt of the negation of MYSN informs the memory that the master has accepted the data. The DR-111 then removes the data from the D lines and negates SSYN. This ends the memory's part of the data transfer cycle.

3.2.1.1.2 Data-Out, DATO or DATOB

Data-Out is defined as a data transfer from a master to the DR-111 memory. DATO and DATOB are Data-Out operations. The timing and protocol for both of these operations are identical.

Figure 3 shows the interaction between master and memory for a typical DATO or DATOB. A bus master places the memory address, the required control bits and the data on the A, C and D Unibus lines. The DR-111 decodes A and C signals to see if it is selected as the slave for this transfer.

The master waits after putting the A, C and D bits on the Unibus. If the previous slave has ended its part of the preceding data cycle by negating SSYN, the master asserts MSYN.

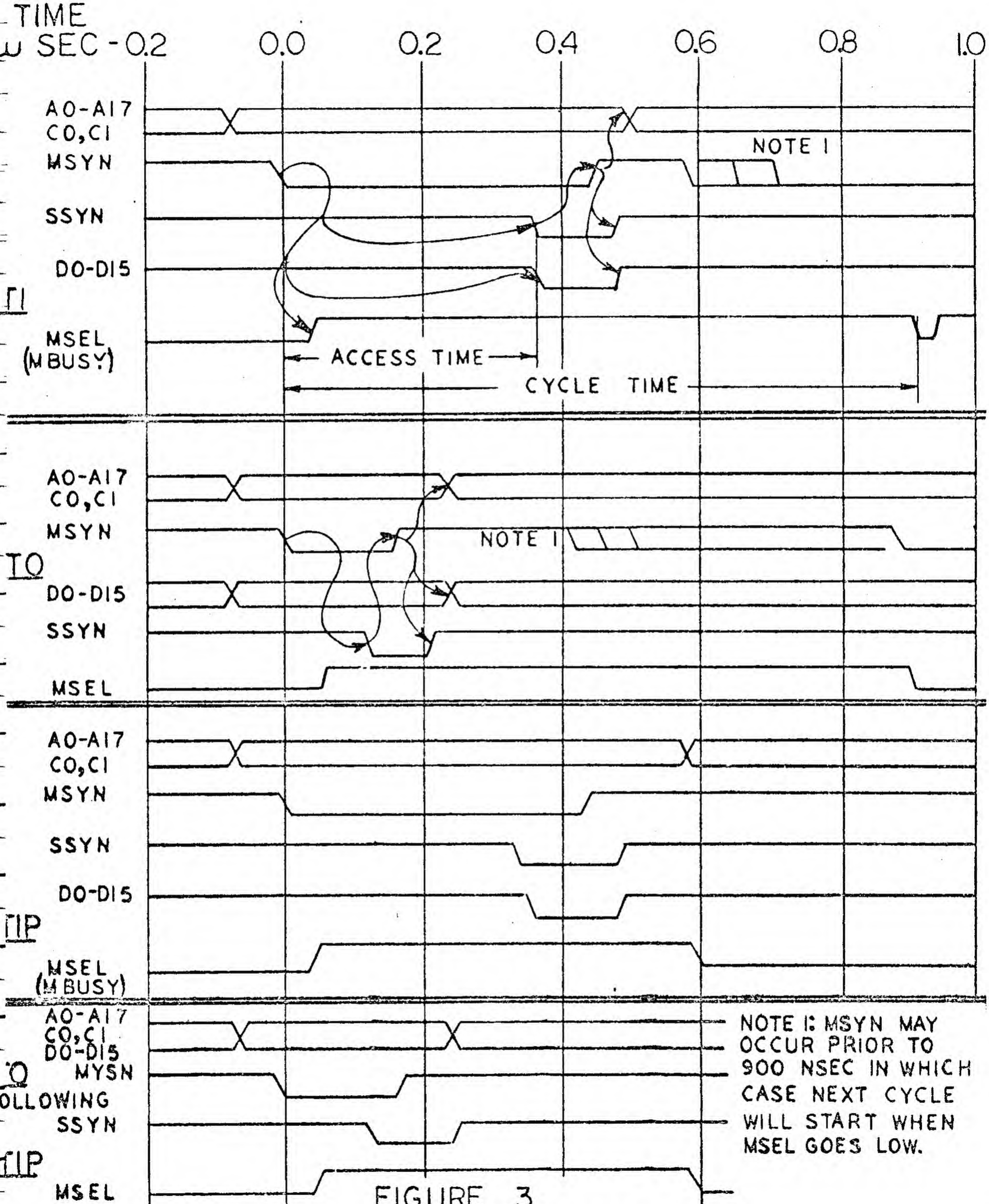
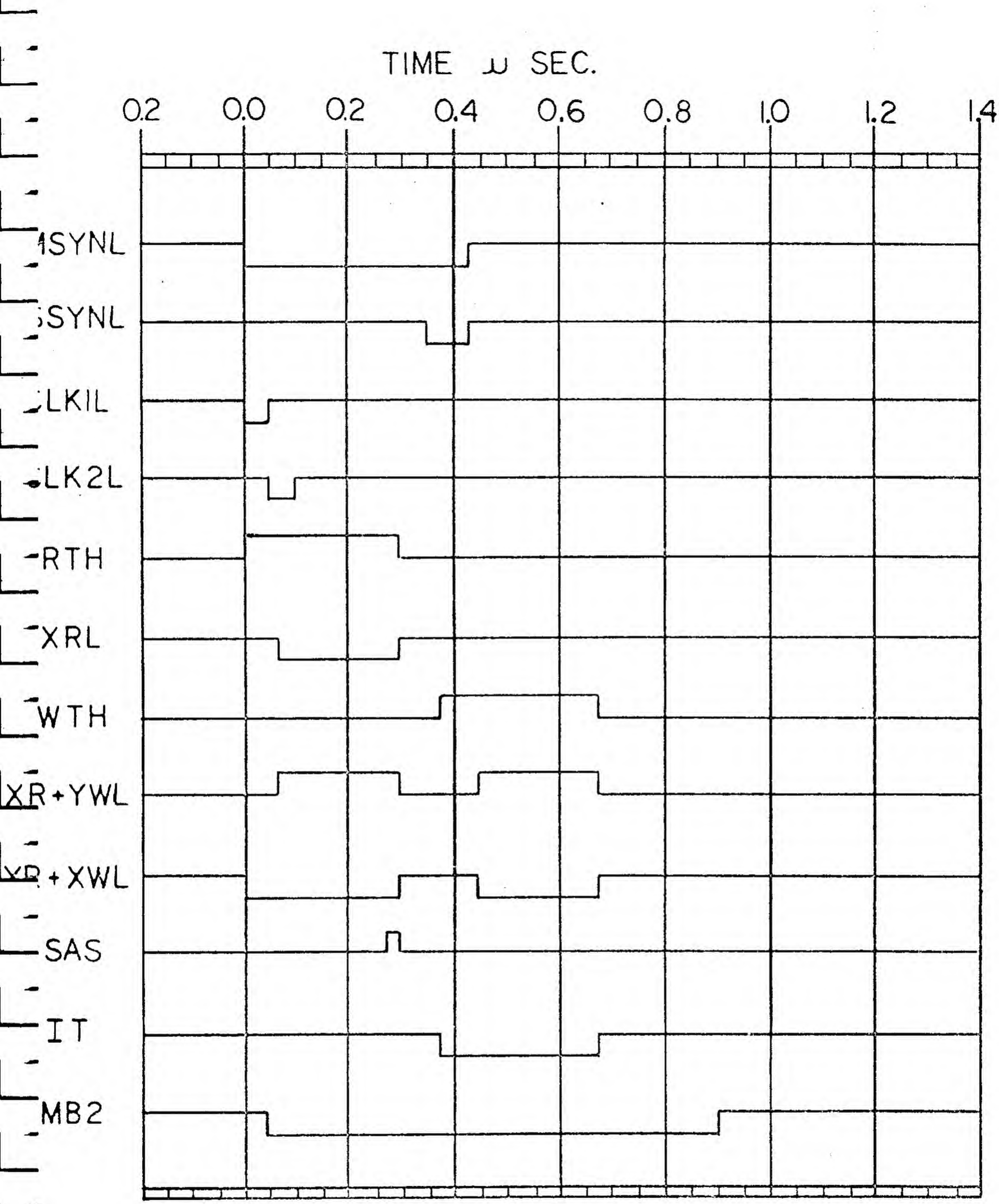


FIGURE 3
TIMING CHART DR-III



DR-111

INTERAL MEMORY TIMING

FIGURE

After receiving the assertion of MSYN, the memory selected as slave strobes the data on the D lines and asserts SSYN.

The master, after receiving the assertion of SSYN, negates MSYN, removes data from the D lines, deskews and removes the A and C bits from their lines.

Upon receipt of the negation of MSYN, the DR-111 ends its part of the data transfer cycle by negating SSYN.

3.2.2 Planar Core Array

The array is of 3D-3 wire organization and uses 18 mil lithium ferrite cores. The X:Y aspect ratio of the array is 128:128 with 8 drives and 16 sinks. Each sense/inhibit line threads through the full complement of 16,384 cores. The sense/inhibit lines are far end terminated with two 100 ohm resistors to ground. The array is driven with positive X and negative Y current during a Read operation and with negative X, positive Y and negative inhibit current during a Write operation. This arrangement of the core array permits a "shared drive" scheme to be used in the DR-111 system minimizing the number of components used and thus improving the system reliability. See Figure 5 for stack pin configuration.

3.2.3 X and Y Current Drive Circuitry (Figures 6, 7, 8 and 9)

Figure 6 depicts the X and Y current scheme used in the DR-111 memory system. The circuitry may be broadly divided into four basic sections:

A. Current Regulator
B. Address Registers
C. Address Decoders
D. Current Switches

3.2.3.1 Current Regulator

The current regulator section consists of two regulated current sources +STAB and -STAB. The +STAB source is used to drive positive current into the stack required by X Read and Y Write operations. The regulation of this source is done at the +5V end of the drive path. The -STAB source drives negative currents from the stack during Y Read and X Write operations and is regulated at the -15V end of the drive path.

Both +STAB and -STAB sources are regulated against a common reference voltage so that the X and Y currents in both the Read and Write operations remain in balance once they have been set. The common reference voltage is controlled by a sensistor which changes its resistance with temperature and causes the drive currents to be compensated for changes in ambient temperature. The drive current is factory set at a level approximately 390mA at +25^{o}C ambient temperature.

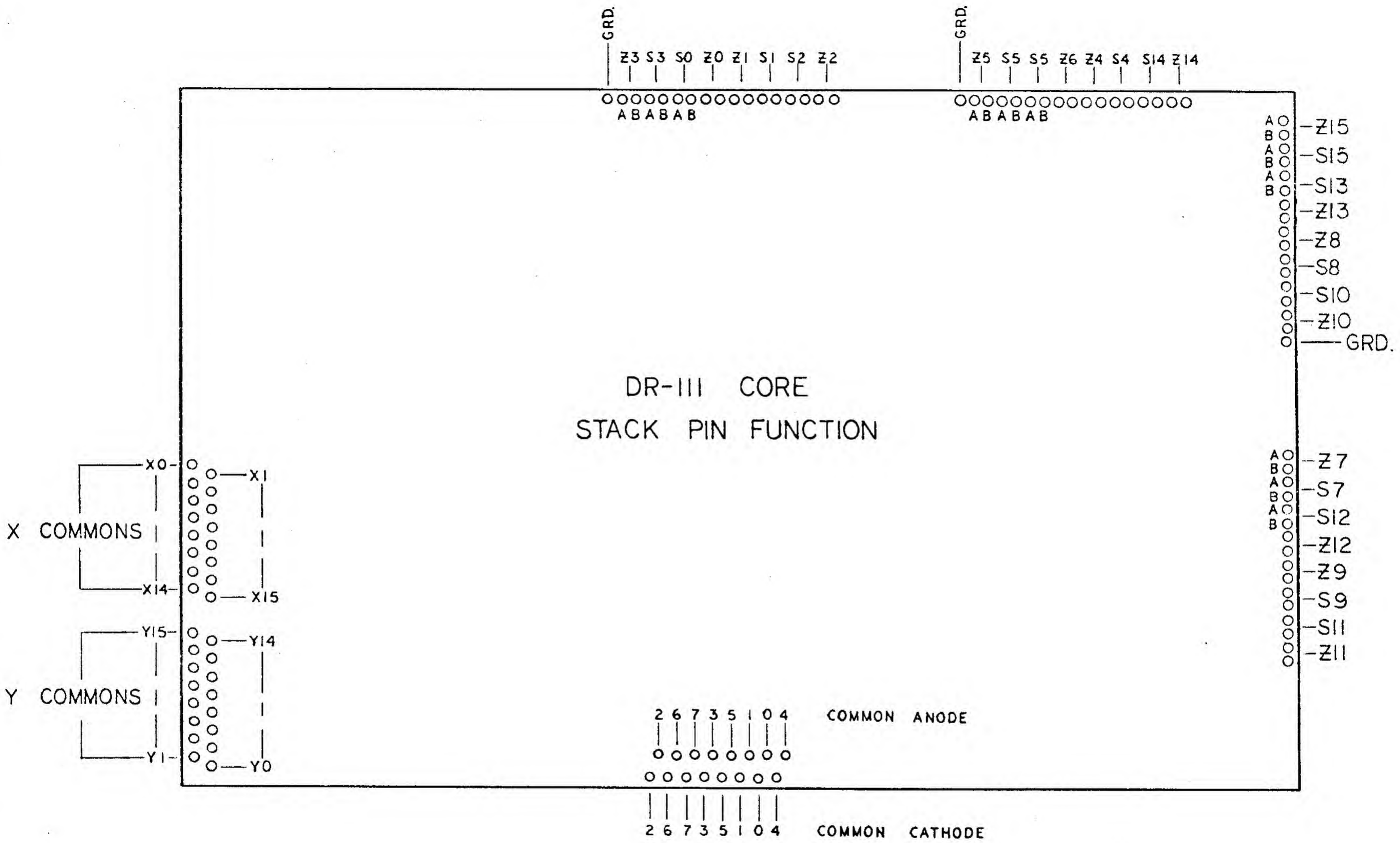

GRD.
Z3 S3 S0 Z0 Z1 S1 S2 Z2
GRD.
Z5 S5 S5 Z6 Z4 S4 S14 Z14
A B A B A B
A B A B A B
Z15
S15
S13
Z13
Z8
S8
S10
Z10
GRD.
DR-III CORE
STACK PIN FUNCTION
X0
X1
X COMMONS
X14
X15
Y15
Y14
Y COMMONS
Y1
Y0
A B A B A B
Z7
S7
S12
Z12
Z9
S9
S11
Z11
2 6 7 3 5 1 0 4
COMMON ANODE
2 6 7 3 5 1 0 4
COMMON CATHODE

FIGURE 5

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

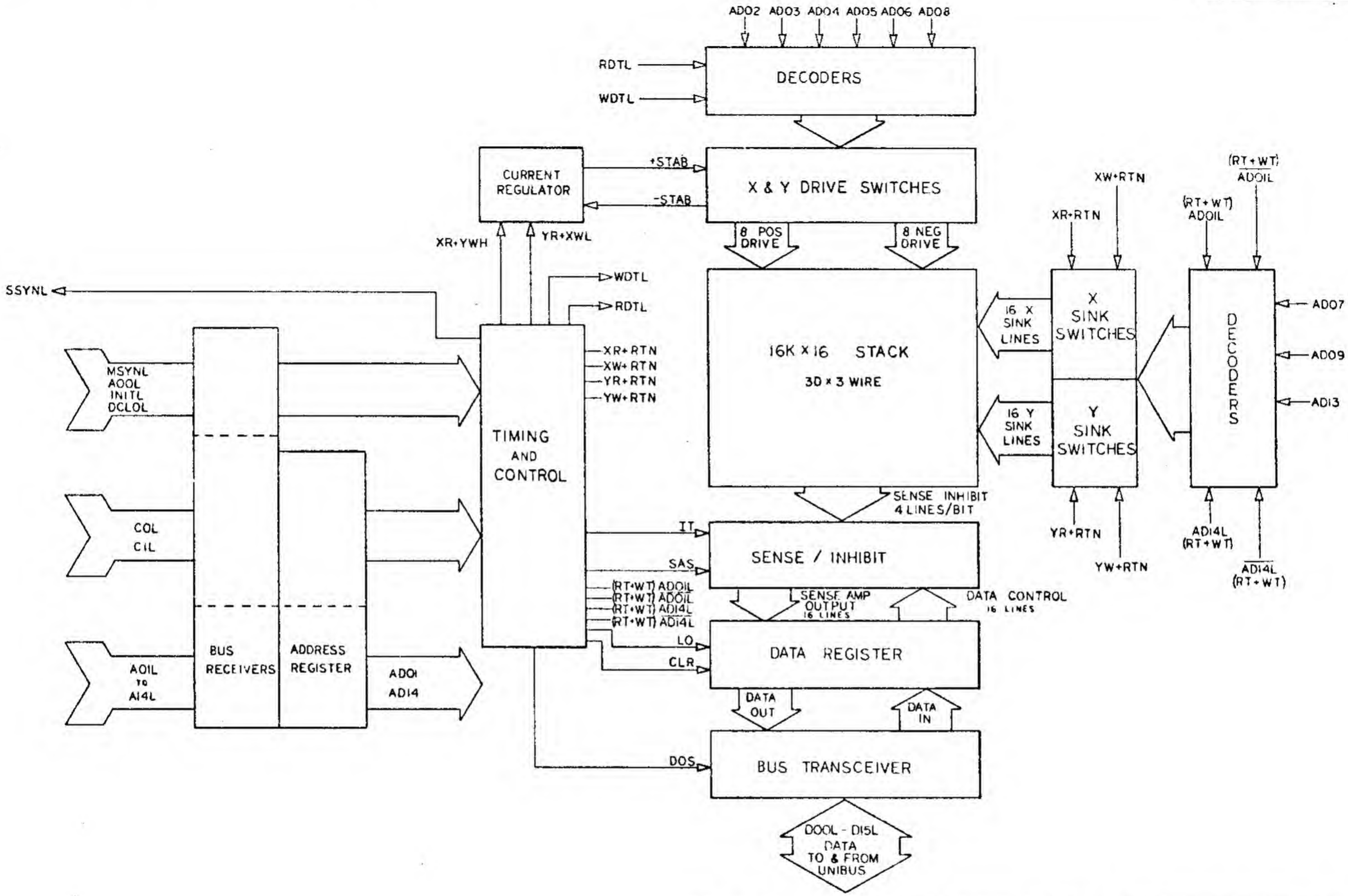


FIGURE 6

NEXT ASSY	USED ON	UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES; TOLERANCES ON: FRACTIONS DECIMALS ANGLES ± .x ± .xx ± ±	DRAWN J. JOHNSON 7-24-75
APPLICATION		MATERIAL	CHECKED / ENGR / APPROVED

DATARAM CORPORATION
CRANBURY NEW JERSEY

DR III
BLOCK DIAGRAM

SIZE	DWG. NO.	REV
D	50473	

SCALE SHEET

WHEN REFERRING TO THIS DRAWING STATE DRAWING NO., APPLICABLE REVISION LETTER IF ANY, AND DATE

3.2.3.2 Address Registers

The address registers store the address information on lines A01 through A14 at the beginning of a memory cycle. The address registers retain this addressing information until the beginning of another Read operation in the memory.

3.2.3.3 Address Decoders

The address decoders convert the address information in the address registers to actual core locations as seen by the memory. The address bits 02, 03 and 04 are decoded to select one of eight Y drive switches while the address bits 07, 09, 13 and 14 are decoded to select one of sixteen Y sink switches. One of eight X drive switches is selected by decoding address bits 08, 05 and 06 and address bits 10, 11, 12 and 01 select one of sixteen X sink switches.

3.2.3.4 Current Switches

All the current switches (including the inhibit switches) used in the DR-111 system are similar in electrical design. All of them are floating switches using a transformer coupled transistor as the switch. The decoders, when activated by the timing pulses, draw current through the primary of the transformer in the selected switch. This primary current induces current in the secondary connected across the base and the emitter of the transistor switching the transistor on.

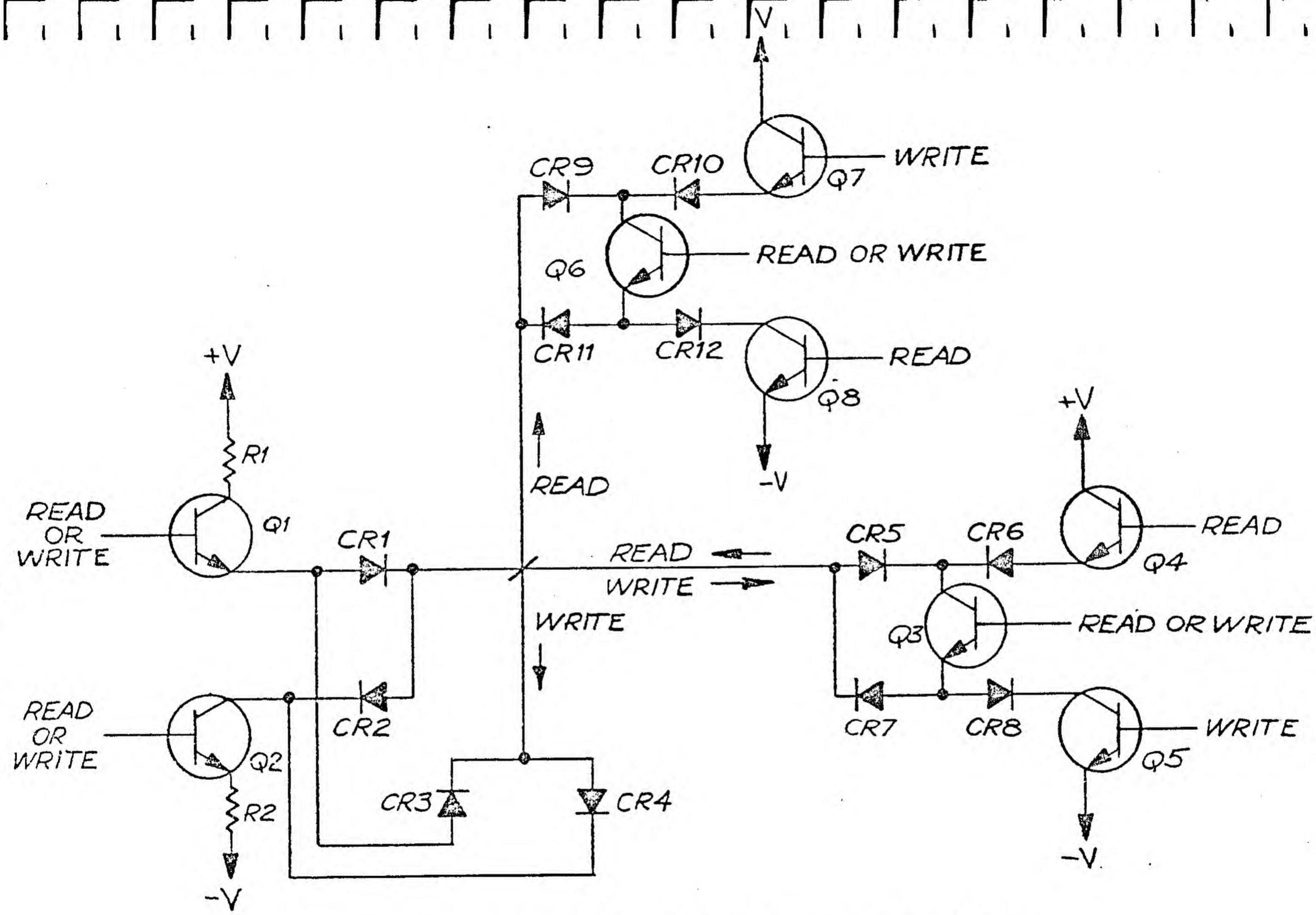
One unique feature of the drive organization is the "shared drive" scheme. The same current switch that drives Y Read current also drives X Write current. Also, one current switch drives both Y Write and X Read current. Thus, by time sharing one current switch between the X and Y dimensions, the DR-111 memory uses only half the drive switches used by a conventional design approach to drive an identical size core array.

Another unique feature of the drive organization is the "bridge sink" scheme. The sink switches are arranged so that a sink node is service by only one sink switch rather than two as in conventional drive schemes. This scheme uses only half the sink switches used by conventional design approaches to drive an identical size core array.

Figure 7 shows a generalized version of this "shared drive-bridge sink" arrangement. A shared drive scheme is shown in which Q_1 supplies current in the Write direction for the X lines and in the Read direction for the Y lines. Transistor Q_2 performs the complementary function by supplying current in the Read direction for the X lines and in the Write direction for the Y lines. Thus, during a Read cycle, Q_2 drives the X lines and Q_1 drives the Y lines. During a Write cycle, Q_1 drives the X lines and Q_2 drives the Y lines.

The direction of current through the drive lines is determined by the bridge switch arrangement on the sink end of the lines. For the X line, this consists of transistors Q3-Q5 and diodes CR5-CR8. Transistor Q_3 is turned on for both the Read and Write cycles. Transistor Q_4 is turned on during the Read cycle only and Q_5 during Write only. Thus, the path for X Read current is through Q_4 , CR6, Q_3 , CR7, Q_2 , and R2. Resistor R2 determines the magnitude of the current. The path for X Write current is through R1, Q_1 , CR1, CR5, Q_3 , CR8 and Q_5. A similar determination establishes the path of current flow in the Y lines.

Figures 8 and 9 show the actual current paths for the DR-111.



SIMPLIFIED DRIVE/SINK SCHEMATIC

FIGURE 7

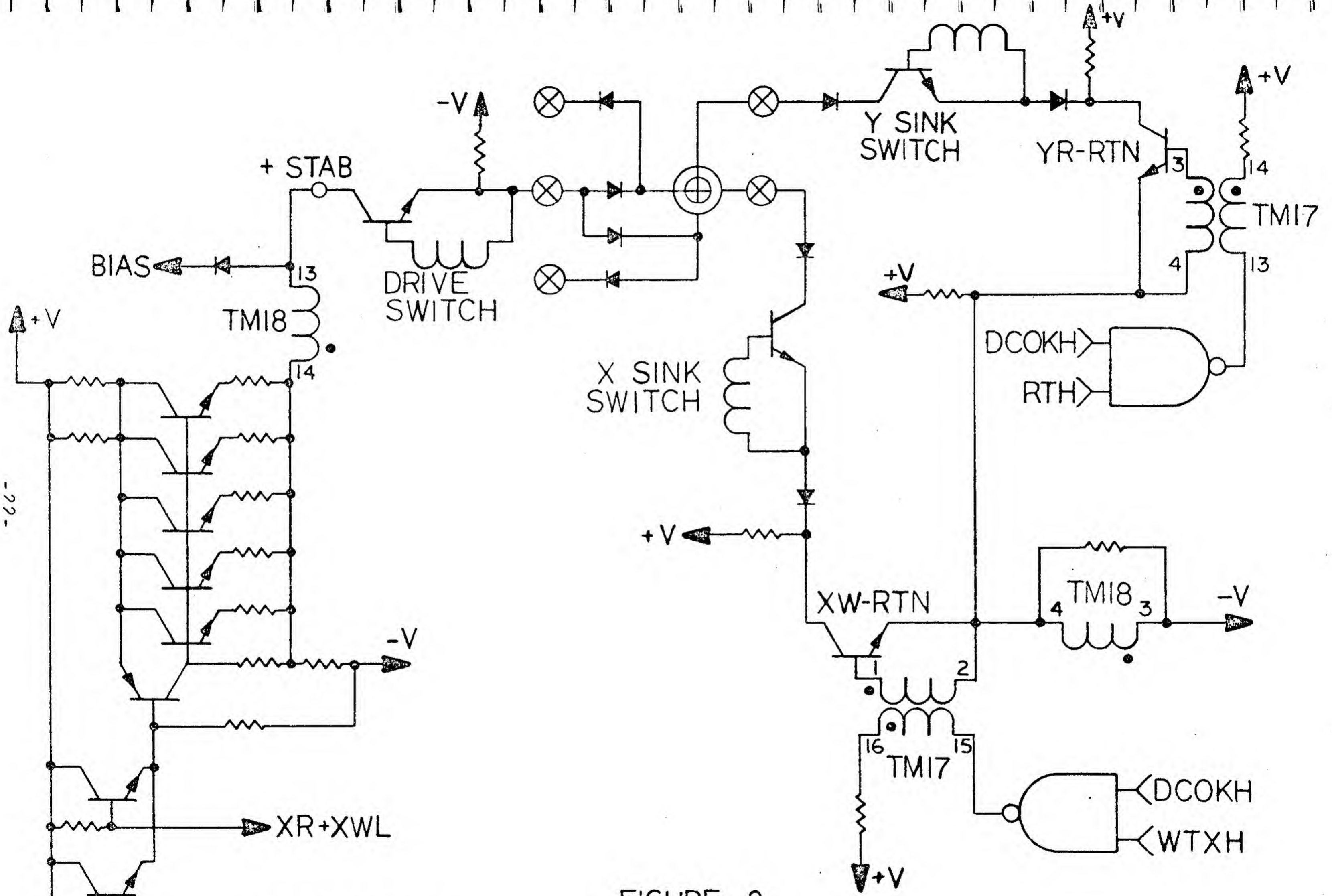


FIGURE 8
TYPICAL YR+XW
DRIVE CIRCUIT

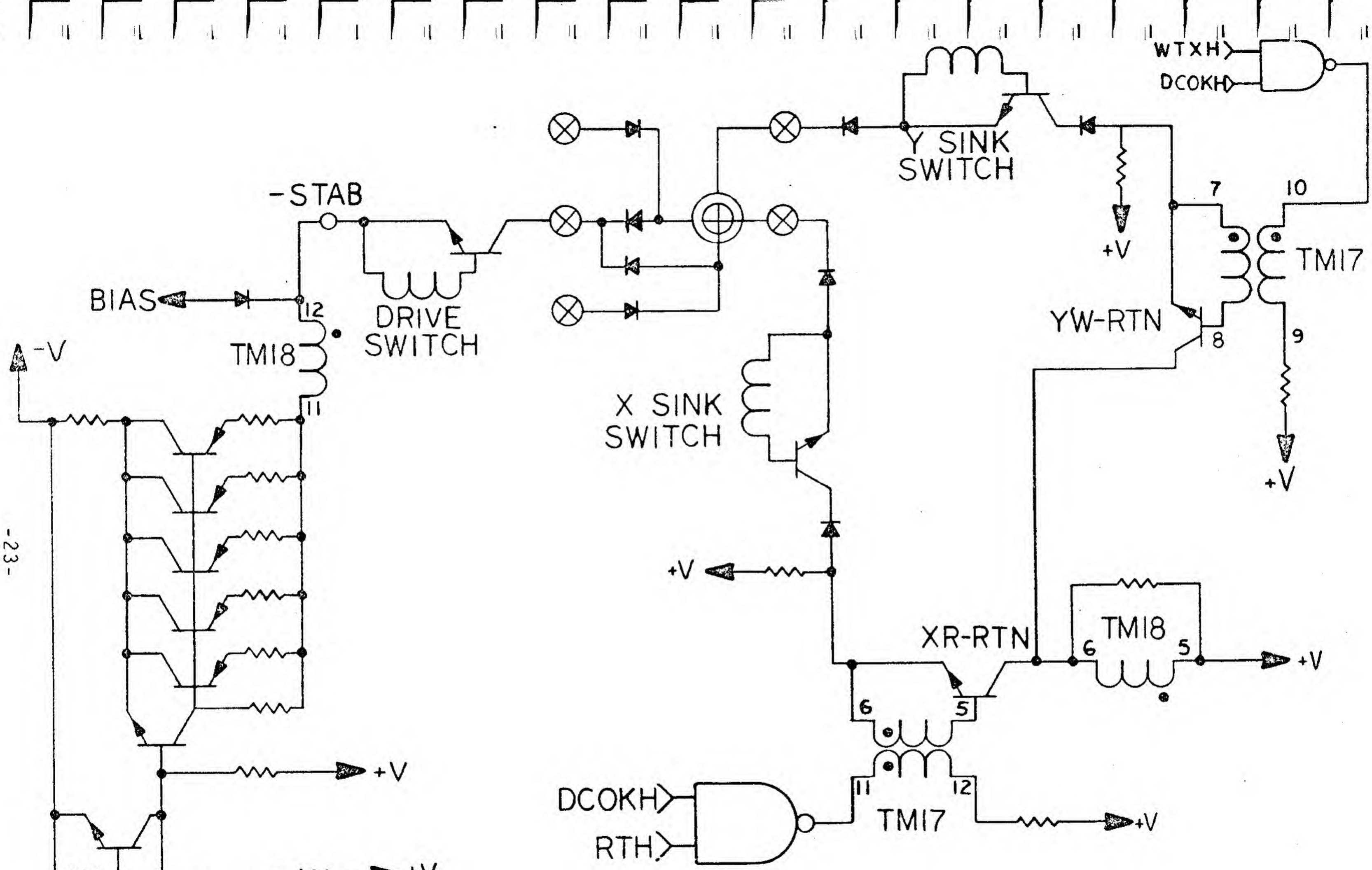


FIGURE 9
TYPICAL XR + YW
DRIVE CIRCUIT

3.2.4 Data Loop Circuitry (Figure 10)

The Data Loop circuitry consists of the Unibus Transceivers, the Data Register, Sense Amplifier and Inhibit Driver. The timing signals required for the Data Loop are generated in the Timing and Control. "IT" is the inhibit timing signal, "VTH" is the Sense Amplifier's threshold voltage, "SAS" is the Sense Amplifier Strobe, "LD" is used to load the data from the Unibus into the Register, "CLR" is used to clear the Register and "DOS" is used to gate the data from the DR-111 onto the Unibus.

A DATO or DATOB cycle clears the register and then loads the data in from the Unibus. During the Clear half cycle, the addressed location is cleared, i.e., the cores are set to zero. During the Write half cycle, the selected address receives a half select current in both the X and Y axis, switching the core to a "1". If a "0" is to be written into a selected core location, the Inhibit Driver is turned on during IT. This inhibit current opposes the Y Write current and the selected core location is left in the "0" state.

A DATI cycle requires reading out of a selected core location and restoring the same information. During the Read half cycle, the data register is first reset. Then the sense amplifier is strobed, approximately during the peak of the core signal, setting the data register if a "1" was present. A "0" signal will not exceed the threshold voltage during the strobe time and, therefore, will leave the data register in the reset state. The strobe adjustment is critical and should only be changed when absolutely necessary. It is set at approximately 350 nanoseconds from MSYNL. The threshold voltage to the sense amplifier is approximately 18 millivolts and is generated by a voltage divider network connected to the VTH supply.

The inhibit driver is a floating transformer coupled transistor switch. The primary is driven from a 75453 integrated circuit. Primary current flows in the transformer when the output from the data register (Data "0") and the inhibit timing signal are both low at the input to the gate.

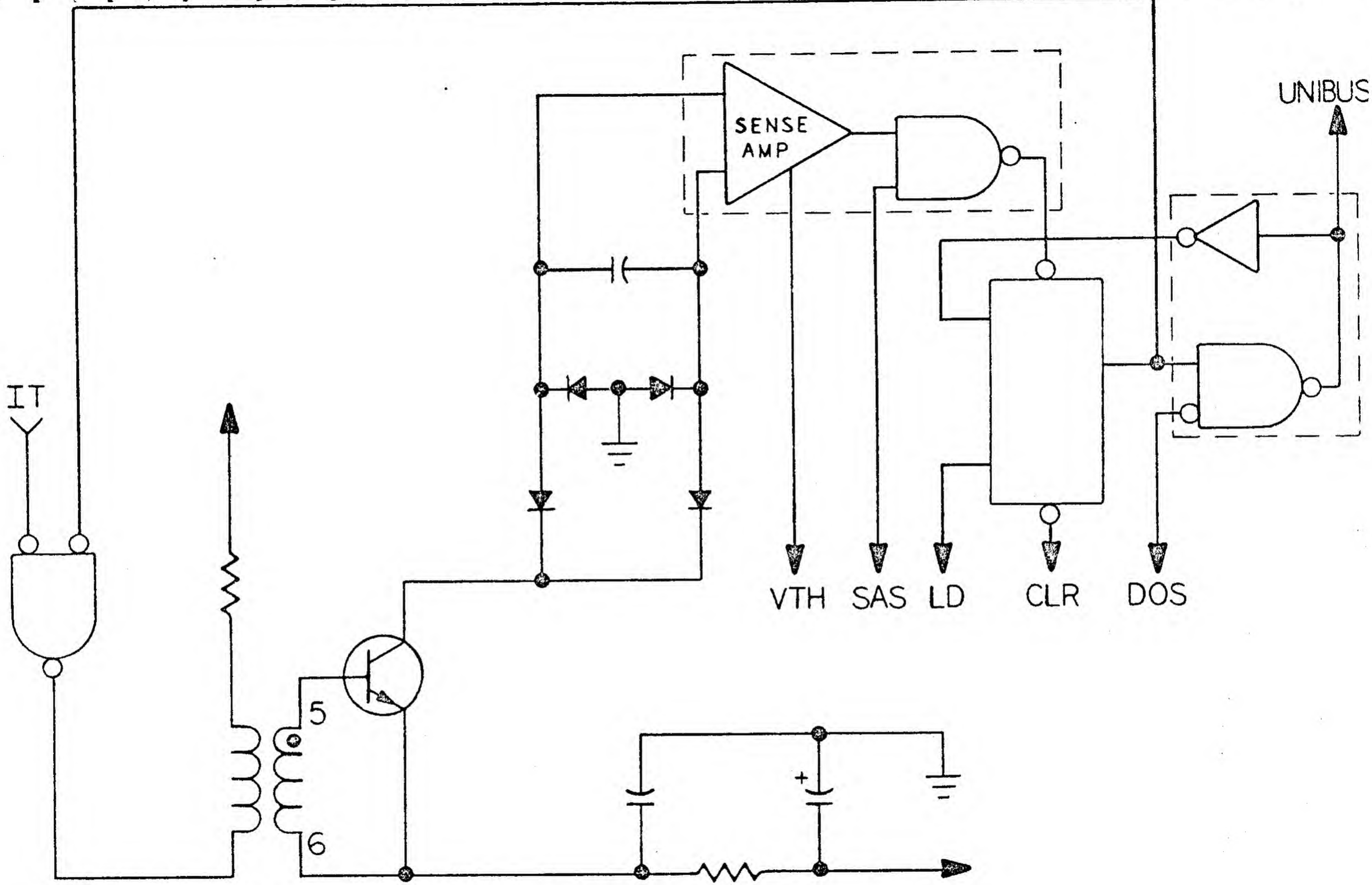
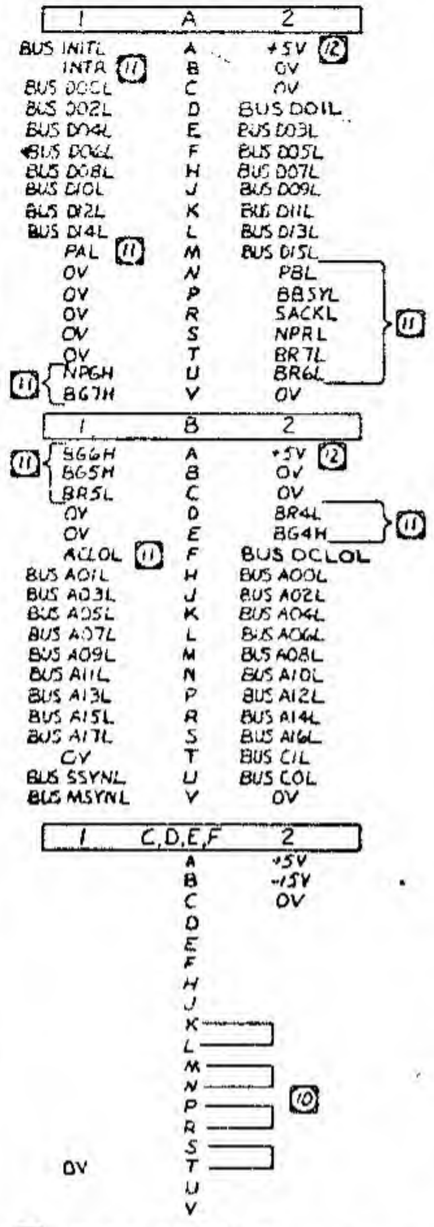
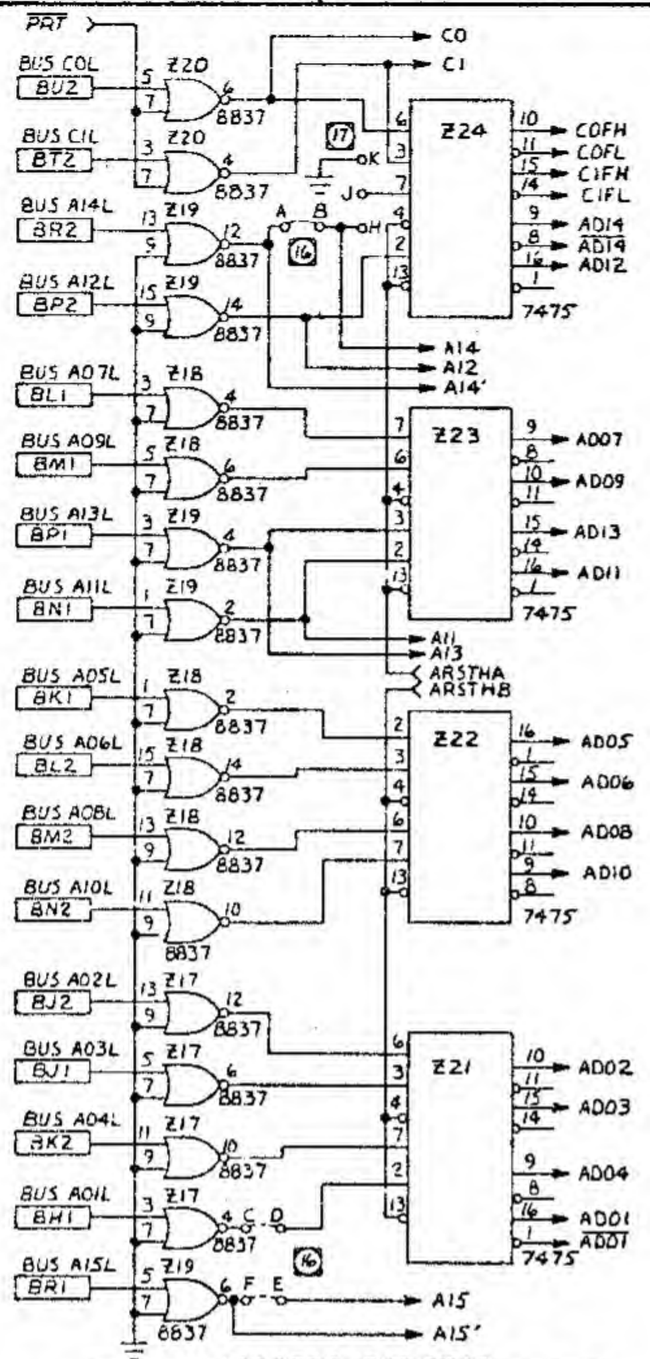


FIGURE 10
TYPICAL SENSE AND DATA LOOP

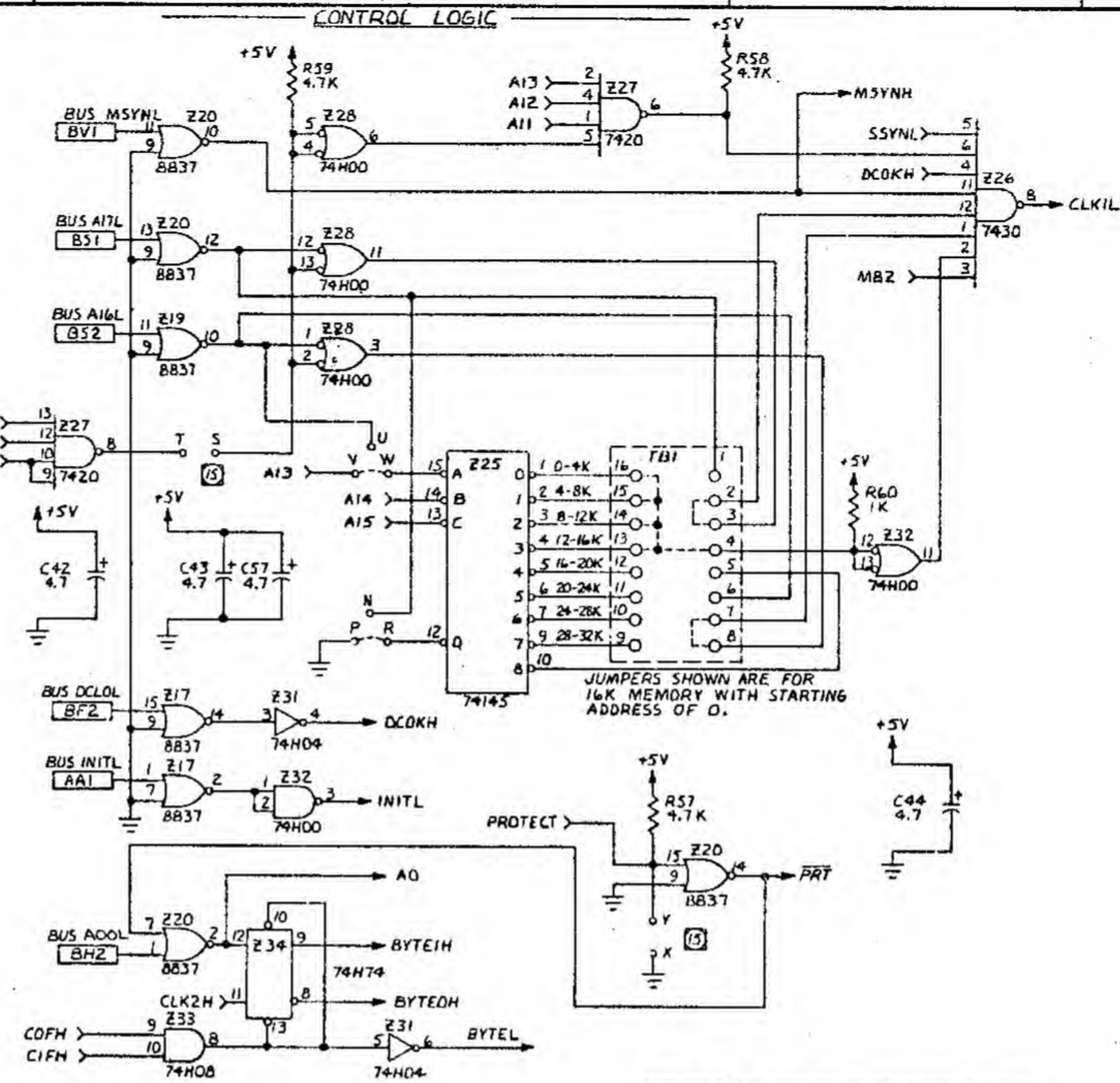
4.0 DOCUMENTATION

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	NC	REL TO PRODUCTION	3-25-75	BP
	A	RELEASED TO DRC PRODUCTION	6-7-75	6-9-BJ
	B	ECN 610	9-17-75	6 VW





ADDRESS REGISTER



AOL	C1L	COL	MODE	DEFINITION
X	H	H	DATI	READ-RESTORE
X	H	L	DATIP	READ
X	L	H	DATO	CLEAR-WRITE
H	L	L	DATOBO	CLEAR WRITE BYTE 0
L	L	L	DATOBI	CLEAR WRITE BYTE 1

(16) NORMAL OPERATION
JUMPER A TO B, V TO W,
C TO D, P TO R,
E TO F

8K INTERLEAVE OPERATION:
JUMPER A TO D
C TO B

16K INTERLEAVE OPERATION:
JUMPER C TO E
F TO D

(17) FOR 16K MEMORY, JUMPER J TO H; K TO J IS OPEN;
FOR 8K MEMORY, JUMPER J TO K; J TO H IS OPEN.

(18) COMPONENTS NOT USED

(19) SELECT VALUE FOR C49 TO OBTAIN 900 TO 925 NS CYCLE TIME.

(15) FOR 31K OPERATION JUMPER S TO T;
FOR MEMORY PROTECT OPERATION, JUMPER X TO Y.

(14) SELECT VALUES FOR R66 AND R70 TO OBTAIN CORRECT PULSE WIDTH PER TEST SPECIFICATION.

(13) SELECT VALUES FOR R154, R157 AND R174 TO OBTAIN 380 MA OF CURRENT IN THE X AND Y DRIVE LINES.

(12) -5V USED FOR TERMINATION ONLY.

(11) SIGNALS ASSIGNED IN UNIBUS BUT NOT USED IN THIS MEMORY.

(10) ON CONNECTOR D ONLY PIN K IS CONNECTED TO L, M TO N, P TO R, AND S TO T; ON BACKSIDE (2).

(9) EXTERNAL POTENTIOMETER USED TO CONTROL X AND Y DRIVE LINES DURING MEMORY TEST.

8. ALL MONOLITHIC TRANSFORMER DEVICES, NOTED TM, ARE 14204 TYPE.
7. ALL MONOLITHIC TRANSISTOR DEVICES, NOTED MHQ, ARE 20401 TYPE.
6. ALL DIODES ARE 1810I TYPE.
5. ALL MONOLITHIC DIODE NETWORKS, NOTED CRU, ARE; CA-18307 TYPE, CC-18308 TYPE.
4. RESISTANCE VALUES ARE IN OHMS, ±5%, 1/4 W.
3. CAPACITANCE VALUES ARE IN MICROFARADS +80-20%.
2. CAPACITANCE TOLERANCE AND VOLTAGES ARE AS FOLLOWS:
MICROFARADS - ± 5%, 100 V; 4.7 MICROFARADS - ± 20%, 10V; 15 MICROFARADS - ± 20%, 20V.
1. FOR ASSEMBLY DRAWING SEE DRAWING NO. 61101.

NOTES: UNLESS OTHERWISE SPECIFIED

TBI (PIN NUMBERS)

INITIAL ADDRESS	MEMORY SIZE	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
0	8K	4	X	X													
	16K	4	X	X	X	X											
	BOTH	2										X				X	
	BOTH	1															
4K	8K	4		X	X												
	16K	4		X	X	X	X										
	BOTH	2										X				X	
	BOTH	1															
8K	8K	4			X	X											
	16K	4			X	X	X	X									
	BOTH	2										X				X	
	BOTH	1															
12K	8K	4				X	X										
	16K	4				X	X	X	X								
	BOTH	2										X				X	
	BOTH	1															
16K	8K	4					X	X									
	16K	4					X	X	X	X							
	BOTH	2										X				X	
	BOTH	1															
20K	8K	4						X	X								
	16K	4						X	X	X	X						
	BOTH	2										X				X	
	BOTH	1															
24K	8K	4							X	X							
	16K	4							X	X	X	X					
	BOTH	2										X				X	
	BOTH	1															

61101	DR-111	UNLESS OTHERWISE SPECIFIED	DATARAM CORPORATION
NEXT ASSY	USED ON	DIMENSIONS ARE IN INCHES	CRANBURY NEW JERSEY
APPLICATION		TOLERANCES ON: FRACTIONS ± DECIMALS .xx ± .xxx ± ANGLES ±	SCHEMATIC DIAGRAM DR-111 MEMORY SYSTEM 16K X 16 BITS
		MATERIAL:	DRAWN M. BOCK 11-22-74; CHECKED 3-24-75; ENG'G 3-24-75; APPROVED B.J.W. 5/27/75
			SIZE D; CODE IDENT NO 50473; DRAWING NO 03059; REV B; SCALE NONE; SHEET 1 OF 8

504033 A

WHEN REFERRING TO THIS DRAWING STATE DRAWING NO., APPLICABLE REVISION LETTER IF ANY, AND DATE

TIMING & CONTROL LOGIC

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

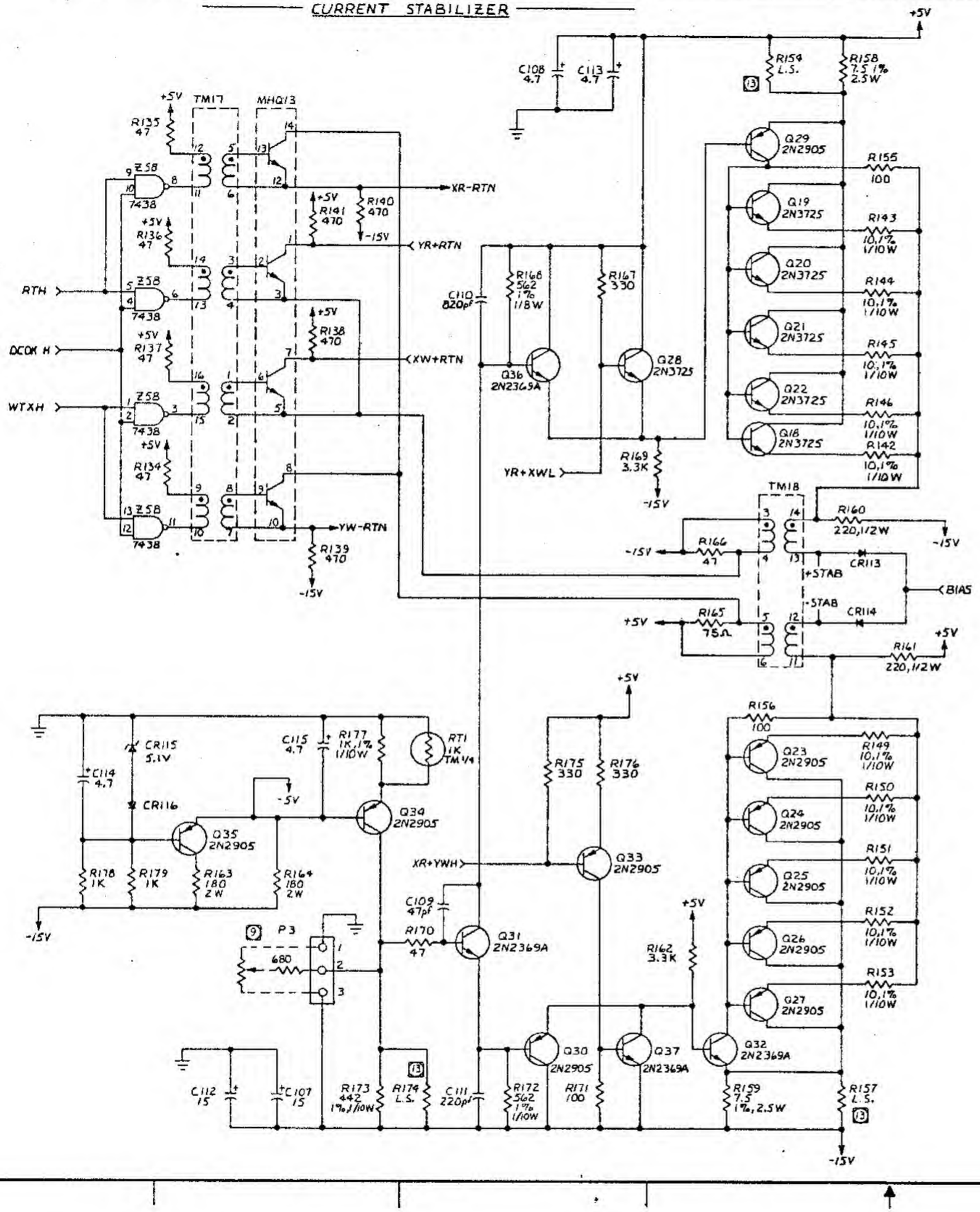
SSYNL
BUS SSYNL
BUI
MSYNH
DOS
BYTEL
BYTEH
SASA
SASB
CIFL
HI-2
CI
CO
AO
CLK2H
CLK2L
CLKIL
CLKIH
LDA
LDB
CLRA
CLRB
PAUSEH
PAUSEL
COFL
COFH
INITL
XRL
RTH
RTL
WTH
WTL
WTXH
WTXL
ADDIL
AD14L
(RT+WT) ADDIL
(RT+WT) AD14L
XR+YWH
YR+XWL
RDTL
WDTL
ITA
ITB
ARSTHA
ARSTHB
MB2
CLK2L
CLK2H
CLKIL
CLKIH
R76 10K CW
R75 4.7K
R74 470
R63 470
R69 10K
R70 L.S.
R46 L.S.
R67 10K
R64 4.7K
R73 2.2K
R72 330
R71 330
R77 330
R61 330
R62 1K
R65 4.7K
R68 220
R180 100Ω
C63 22pf
C62 10pf
C53 100pf
C55 100pf
C52 100pf
C54 22pf
C51 220pf
C48 10pf
C45 4.7
C56 4.7
C50 4.7
C64 10pf
C47 100pf
C46 100 pf
C49 S.A.T.
L2 22µh
L3 22µh
Z57 74123
Z42 74123
Z36 74123
Z34 74H74
Z30 74H74
Z37 74S51
Q9 2N2369A

61101	DR-III	UNLESS OTHERWISE SPECIFIED	DATARAM CORPORATION, CRANBURY, NEW JERSEY
NEXT ASSY	USED ON	DIMENSIONS ARE IN INCHES	SCHEMATIC DIAGRAM
APPLICATION		TOLERANCES ON: FRACTIONS ± DECIMALS .xx ± .xxx ± ANGLES ±	DR-III MEMORY SYSTEM 16K x 16BITS
		MATERIAL:	DRAWN M.BOCK 11-22-76; CHECKED D.HEIFFER 12-24-76; ENGR Y.Yaffa 3-25-77; APPROVED
			SIZE D; DOCUMENT NO 50473; DRAWING NO 030359; REV B; SCALE NONE; SHEET 2 OF 8

504033 A

WHEN REFERRING TO THIS DRAWING STATE DRAWING NO., APPLICABLE REVISION LETTER (IF ANY), AND DATE

CURRENT STABILIZER



LAST DESIGNATION USED	
RESISTOR	R181
CHOKE	L3
RESISTOR MODULE	RM21
TRANSISTOR	Q37
CAPACITOR	C115
DIODE MODULE	CRM12
DIODE	CR116
INTEGRATED CIRCUIT	Z70
TRANSISTOR MODULE	MHQ13
THERMISTOR	RT1
TRANSFORMER MODULE	TM18

REF DESIG	GATES USED PER TOTAL	PART NUMBER
Z28	3/4	74H00
Z31	4/6	74H04
Z32	3/4	74H00
Z33	3/4	74H08
Z39	2/3	74H10
Z41	4/6	74H04
Z53	2/4	7438
Z55	3/4	74H00
TM18	2/4	14204

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

		UNLESS OTHERWISE SPECIFIED
		DIMENSIONS ARE IN INCHES
		TOLERANCES ON:
		FRACTIONS DECIMALS ANGLES
		± .xx ± ±
		.xxx ±
		MATERIAL:
G1101	DR-111	
NEXT ASSY	USED ON	
APPLICATION		

DRAWN	M.BOCK	DATE 11-22-74
CHECKED		2-24-75
ENGR		3-25-75
APPROVED		

DATARAM CORPORATION
CRANBURY NEW JERSEY

SCHEMATIC DIAGRAM
DR-111 MEMORY SYSTEM
16K x 16 BITS

SIZE	CODE IDENT NO	DRAWING NO	REV
D	50473	030519	B

SCALE NONE SHEET 3 OF 8

504033 A

WHEN REFERRING TO THIS DRAWING STATE DRAWING NO., APPLICABLE REVISION LETTER IF ANY, AND DATE

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

Y SINK

X SINK

X & Y DRIVE

		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON: FRACTIONS DECIMALS ANGLES ± XX ± ± XXX ±	DRAWN M.SOCK 11-22-74 CHECKED D.FEIFFER 3-24-75 ENGR D.Tate 3-25-75 APPROVED
61101	DR-111	MATERIAL:	
NEXT ASSY	USED ON		
APPLICATION			

DATARAM CORPORATION
CRANBURY N.J.

SCHEMATIC DIAGRAM
DR-111 MEMORY SYSTEM
16K x 16 BITS

SIZE	CODE IDENT NO	DRAWING NO	REV
D	50473	03059	B

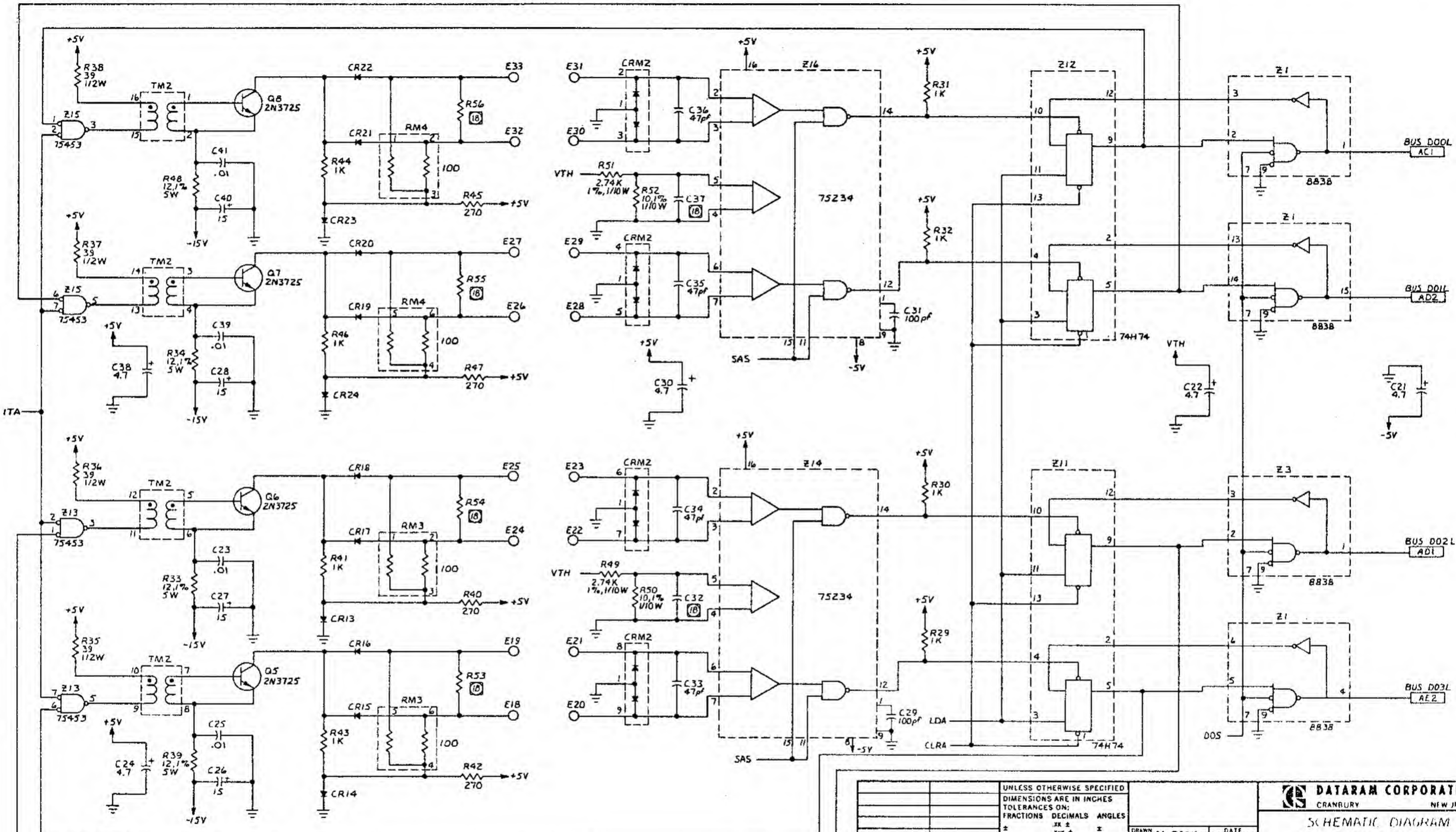
SCALE NONE SHEET 1 OF 1

504033 A

WHEN REFERRING TO THIS DRAWING STATE DRAWING NO., APPLICABLE REVISION LETTER IF ANY, AND DATE

SENSE INHIBIT

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		



		UNLESS OTHERWISE SPECIFIED	
		DIMENSIONS ARE IN INCHES	
		TOLERANCES ON:	
		FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±	
		MATERIAL:	
61101	DR-111		
NEXT ASSY	USED ON		
APPLICATION			

DRAWN	M. BOCK	DATE 11-22-74
CHECKED	B. HEITER	2-24-75
ENGR		
APPROVED		

DATARAM CORPORATION
CRANBURY NEW JERSEY

SCHEMATIC DIAGRAM
DR-III MEMORY SYSTEM
16K x 16 BITS

SIZE	CODE IDENT NO	DRAWING NO	REV
D	50473	03059	B

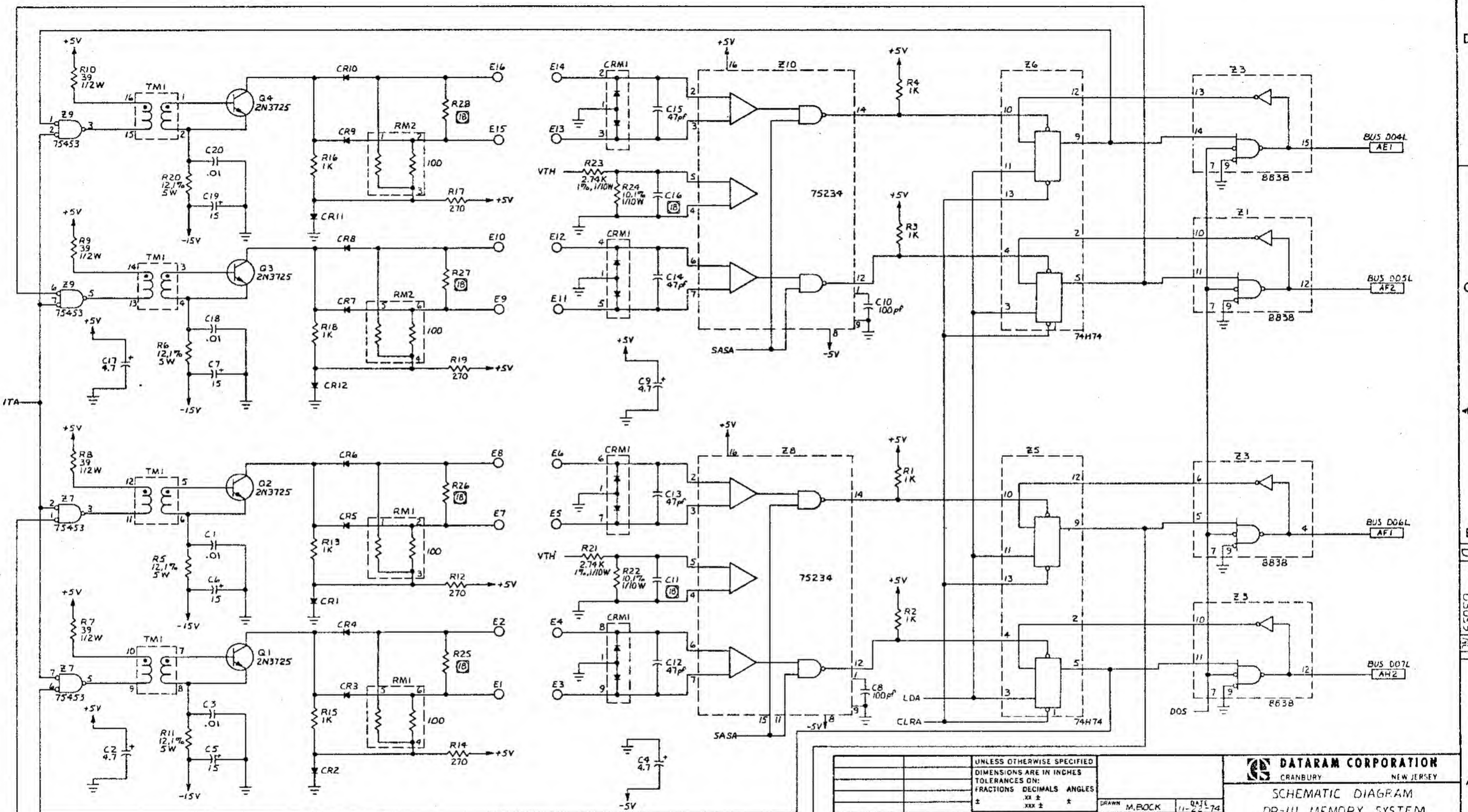
SCALE NONE SHEET 3 OF 11

504033 A

WHEN REFERRING TO THIS DRAWING STATE DRAWING NO., APPLICABLE REVISION LETTER IF ANY, AND DATE

SENSE INHIBIT

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		



		UNLESS OTHERWISE SPECIFIED	DATARAM CORPORATION
		DIMENSIONS ARE IN INCHES	CRANBURY NEW JERSEY
		TOLERANCES ON: FRACTIONS ± DECIMALS .xx ± .xxx ± ANGLES ±	SCHEMATIC DIAGRAM DR-III MEMORY SYSTEM 16K x 16 BITS
6/101	DR-III	MATERIAL:	DRAWN M.BOCK 11-26-74
NEXT ASSY	USED ON		CHECKED 3-24-75
APPLICATION			ENGR 3-25-75
			APPROVED

SIZE	CODE IDENT NO	DRAWING NO	REV
D	50473	03059	B

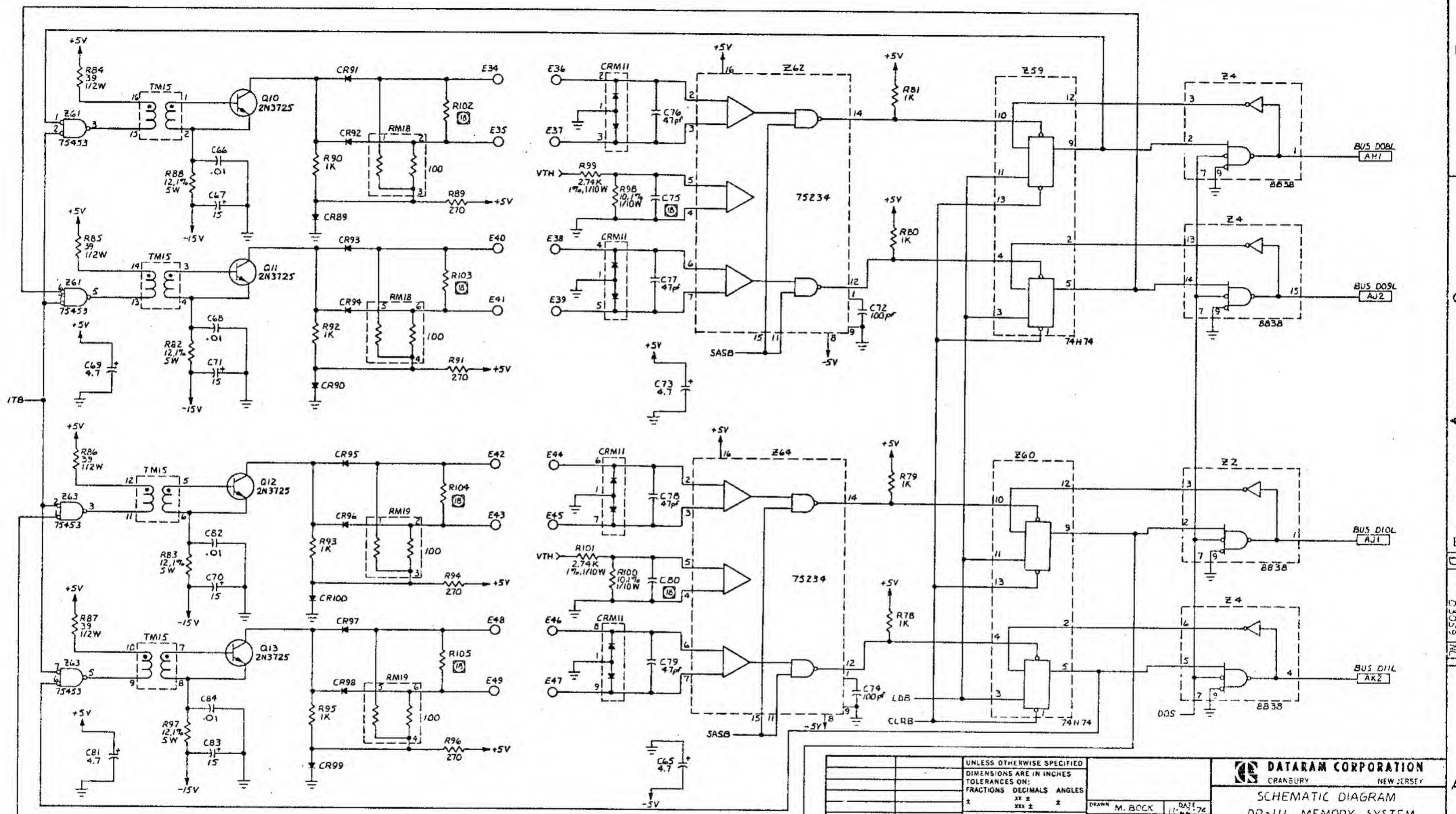
SCALE NONE SHEET 6 OF 8

504033 A

WHEN REFERRING TO THIS DRAWING STATE DRAWING NO., APPLICABLE REVISION LETTER IF ANY, AND DATE

SENSE INHIBIT

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		



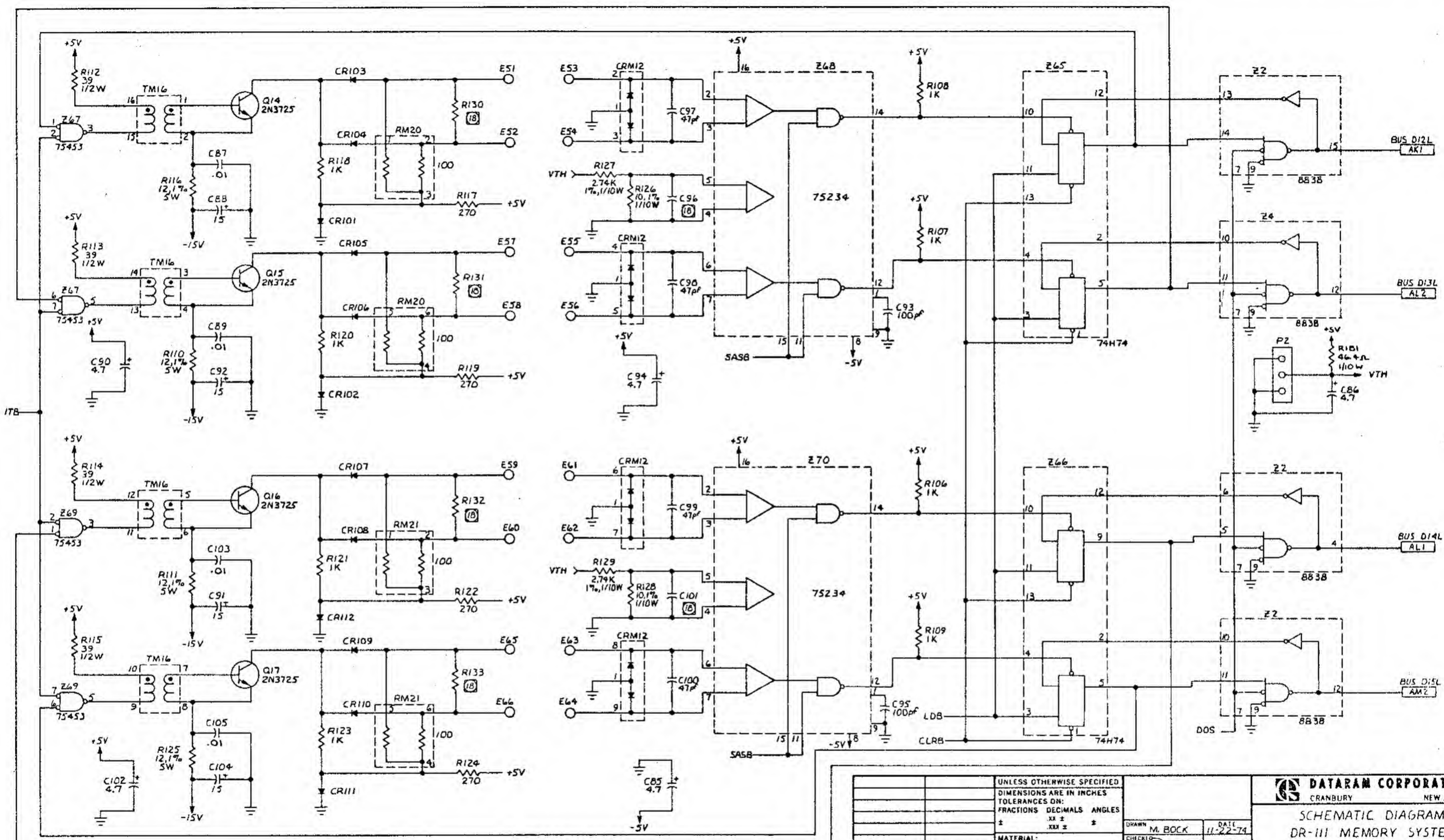
		UNLESS OTHERWISE SPECIFIED		DATARAM CORPORATION	
		DIMENSIONS ARE IN INCHES		CRANBURY	NEW JERSEY
		TOLERANCES ON:		SCHEMATIC DIAGRAM	
		FRACTIONS DECIMALS ANGLES		DR-111 MEMORY SYSTEM	
		± .XX ± .XXX ± ±	DRAWN M. BOCK 11-22-74	16K x 16BITS	
		MATERIAL:	CHECKED B. PFEIFFER 2-26-75		
			ENGR J. Catalano 2-25-75		
61101	DR-111		APPROVED	SIZE D	CODE IDENT NO 50473
NEXT ASSY	USED ON			DRAWING NO 03059	REV B
APPLICATION				SCALE NONE	SHEET 7 OF 8

504033 A

WHEN REFERRING TO THIS DRAWING STATE DRAWING NO., APPLICABLE REVISION LETTER IF ANY, AND DATE

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

SENSE INHIBIT



61101	DR-111
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±
MATERIAL:

		DATE
DRAWN	M. BOCK	11-22-74
CHECKED	D. PFEIFFER	3-24-75
ENGR		
APPROVED		

DATARAM CORPORATION
CRANBURY NEW JERSEY

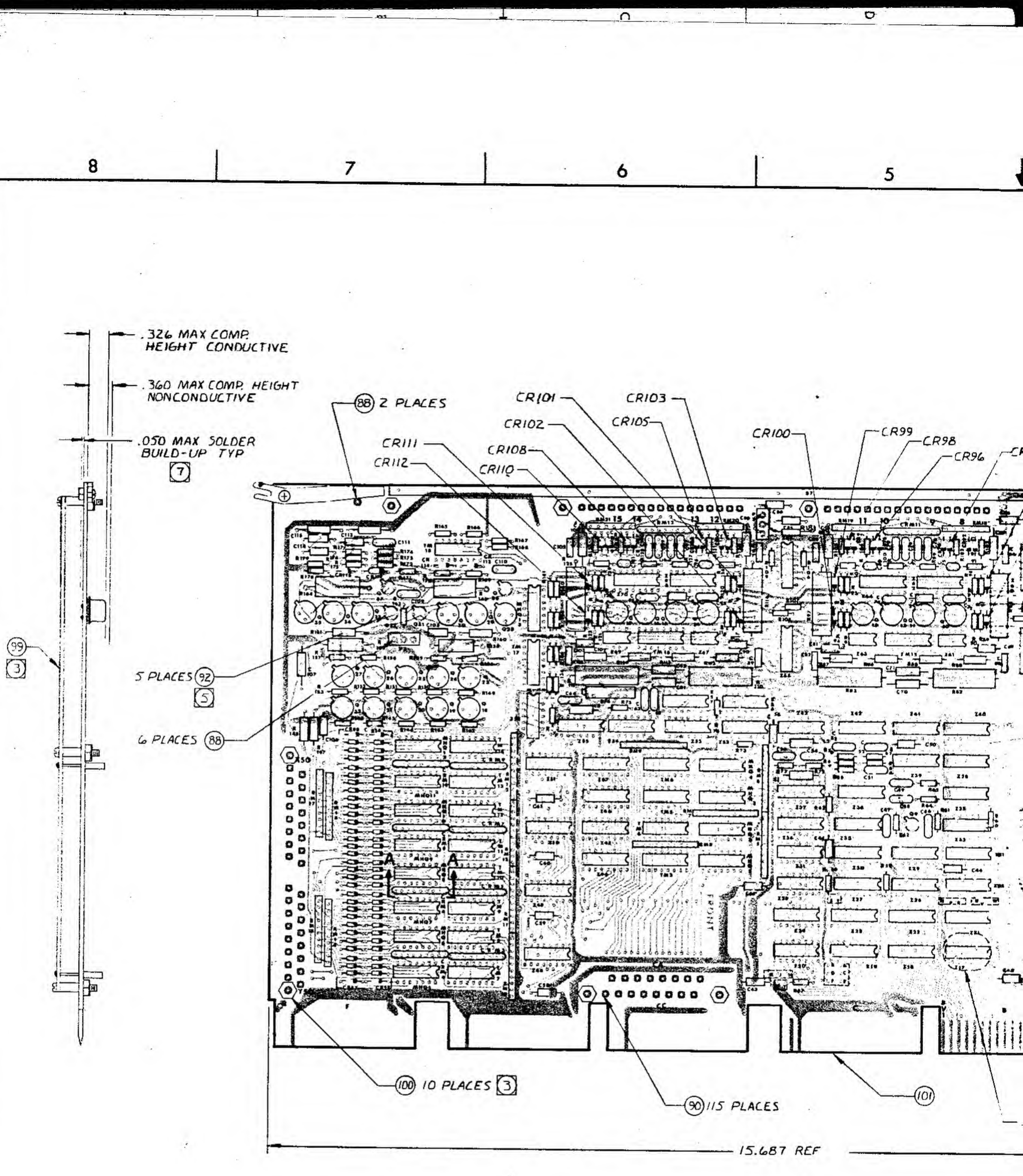
SCHEMATIC DIAGRAM
DR-111 MEMORY SYSTEM
16K x 16 BITS

SIZE	CODE IDENT NO	DRAWING NO	REV
D	50473	03059	H

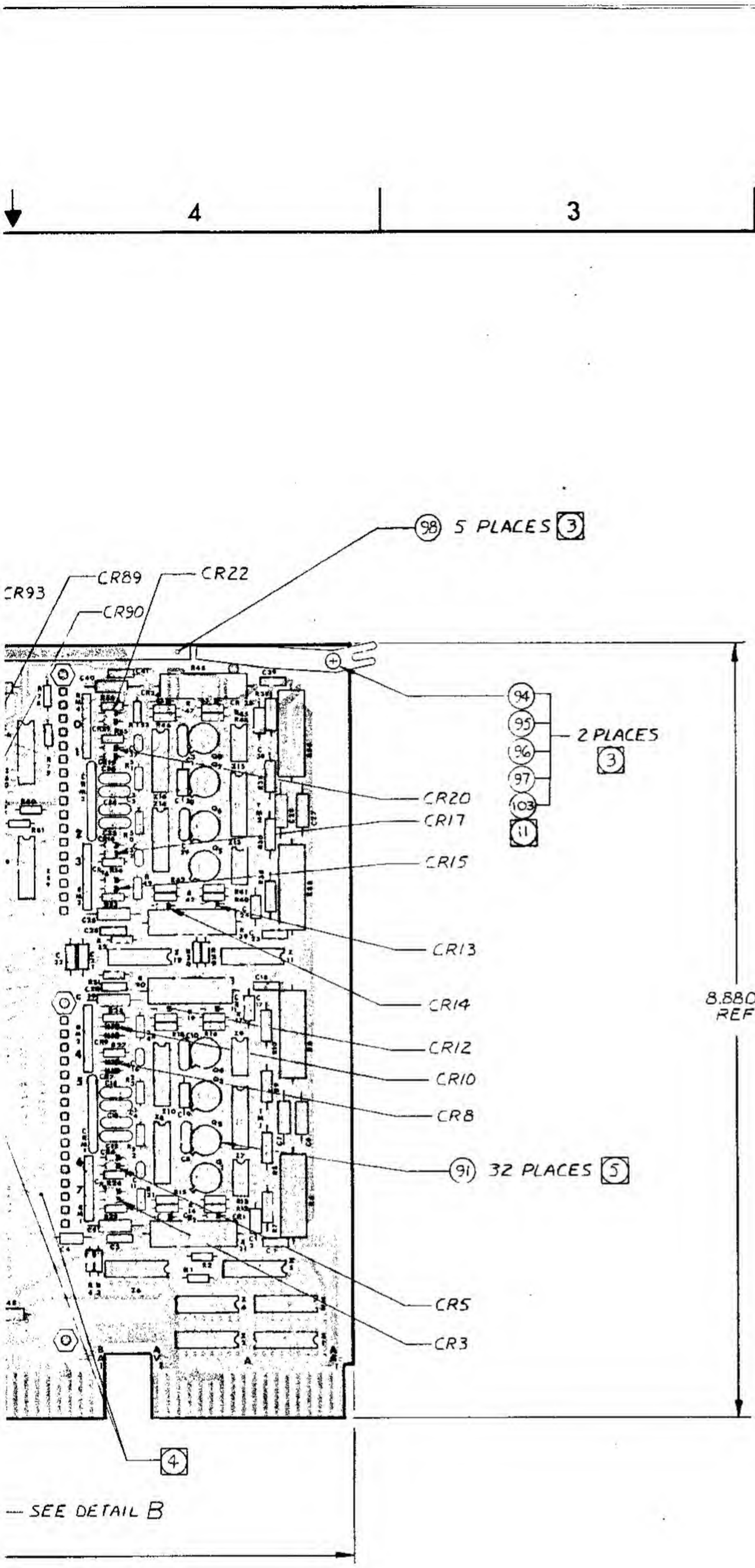
SCALE NONE SHEET 1 OF 4

504033 A

WHEN REFERRING TO THIS DRAWING STATE DRAWING NO., APPLICABLE REVISION LETTER IF ANY, AND DATE


8
7
6
5
D
C
B
A
.326 MAX COMP. HEIGHT CONDUCTIVE
.360 MAX COMP. HEIGHT NONCONDUCTIVE
.050 MAX SOLDER BUILD-UP TYP
7
88 2 PLACES
CR101
CR103
CR102
CR105
CR100
CR99
CR98
CR96
CR111
CR108
CR112
CR110
99
3
5 PLACES 92
5
6 PLACES 88
100 10 PLACES 3
90 115 PLACES
101
FRONT
15.687 REF
PIN NO. 1
.04 MAX
SECTION A-A SCALE 2:1
TYP DIODE MODULE MOUNTING
8 7 6 5 4 3 2 1
9 10 11 12 13 14 15 16
DETAIL B SC
TYP PIN ORIENTAT
INTEGRATED CIRCU
PINS) TM'S, MHG'S
BRUNING 40-107 18156

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	NC	REL TO PRODUCTION	3-25-75	BP
	A	REL TO DRC PRODUCTION	4-22-75	GYW
	B	ECN 571, 610	9-17-75	GYW
	C	ECN 610A	9-17-75	GYW
	D	ECN 639A	9-17-75	GYW
	E	ECN 657A	11-11-75	GYW
	F	ECN 697	12-3-75	GYW



NOTES: UNLESS OTHERWISE SPECIFIED

1. FOR SCHEMATIC DIAGRAM SEE DRAWING NO.
2. COMPONENT DESIGNATIONS ARE FOR REFERENCE PURPOSES ONLY AND DO NOT APPEAR ON COMPONENT PART.
3. INSTALL AFTER FLOW SOLDER.
4. MARK LATEST REVISION LETTER, SERIAL NO. AND EIA DATE CODE WITH .12 HIGH CHARACTERS USING BLACK INK PER MIL-M-13231, GROUP III. LOCATION APPROXIMATELY AS SHOWN.
5. TRANSIPAD (ITEMS 91 AND 92) TO BE INSTALLED UNDER TRANSISTORS (TO-5 AND TO-18) PRIOR TO INSTALLING ON BOARD.
6. ALL COMPONENTS TO BE MOUNTED IN ACCORDANCE WITH DATARAM QC SPEC. 2QC2000.
7. COMPONENT LEAD TRIM AND SOLDER BUILD-UP AS NOTED.
8. RAISE RESISTORS OVER 1/2 WATT OFF BOARD TO .360 MAX HEIGHT.
9. ITEM 102 TO BE INSTALLED AFTER ITEM 89.
10. WIRE-WRAP USING #30 AWG (PN24305) A TO B, C TO D, E TO F, V TO W, P TO R & J TO H.
11. ITEM 103 TO BE INSTALLED BETWEEN P.C. BOARD & EXTRACTOR.

PIN NO.1 TAB
FRONT AND BACK

SCALE 2:1
TATION FOR
RCUITS (14 AND 16
3'S AND TBI.

		UNLESS OTHERWISE SPECIFIED
		DIMENSIONS ARE IN INCHES
		TOLERANCES ON:
		FRACTIONS ± DECIMALS xx ± .02 xxx ± .010 ANGLES ±
		MATERIAL:
	DR-111	
NEXT ASSY	USED ON	
APPLICATION		

DRAWN	M. BOCK	DATE 3-20-75
CHECKED	B. PFEIFFER	3-25-75
ENGR.		
APPROVED	BPH	4/22/75

DATARAM CORPORATION
CRANBURY NEW JERSEY

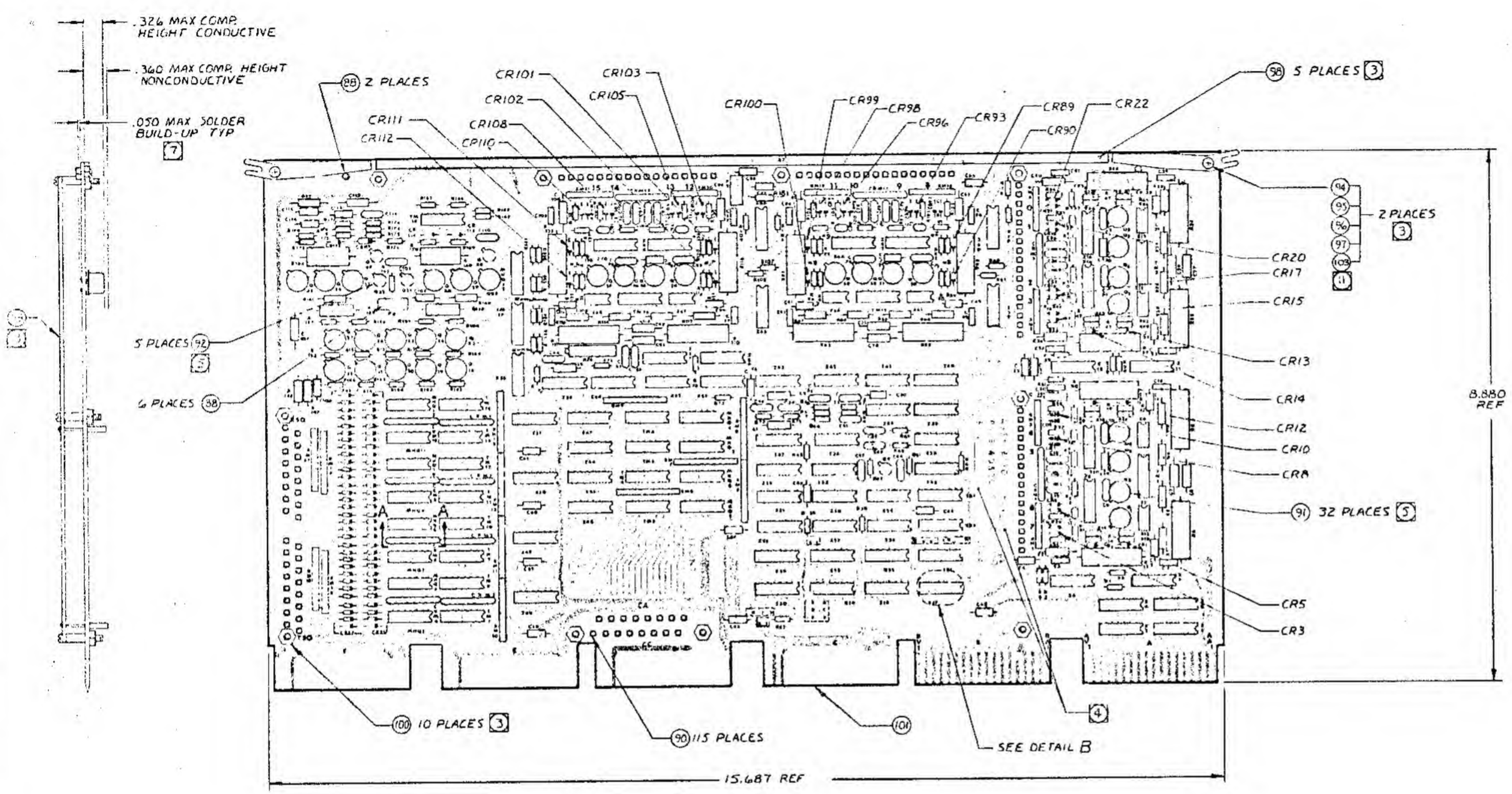
ASSEMBLY
DR-111 MEMORY SYSTEM
16K x 16BITS

SIZE	CODE IDENT. NO.	DRAWING NO.	REV.
D	50473	61101	F

SCALE 1/1 SHEET 1 OF 2

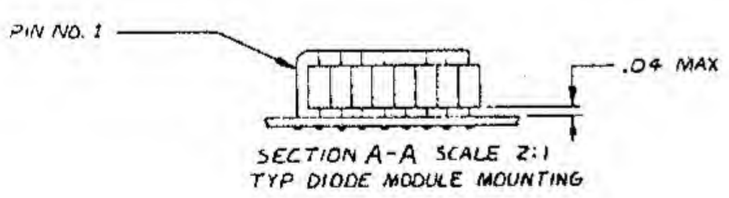
WHEN REFERRING TO THIS DRAWING STATE DRAWING NO., APPLICABLE REVISION LETTER IF ANY, AND DATE

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	NC	REL TO PRODUCTION	3-25-75	BP
	A	REL TO DRC PRODUCTION	4-22-75	GYW
	B	ECN 571, 610	9-11-75	GYW
	C	ECN 610A	9-11-75	GYW
	D	ECN 634A	9-12-75	GYW
	E	ECN 657A	11-11-75	GYW
	F	ECN 697	12-31-75	GYW



NOTES: UNLESS OTHERWISE SPECIFIED

1. FOR SCHEMATIC DIAGRAM SEE DRAWING NO.
2. COMPONENT DESIGNATIONS ARE FOR REFERENCE PURPOSES ONLY AND DO NOT APPEAR ON COMPONENT PART.
3. INSTALL AFTER FLOW SOLDER.
4. MARK LATEST REVISION LETTER, SERIAL NO. AND EIA DATE CODE WITH .12 HIGH CHARACTERS USING BLACK INK PER MIL-M-13231, GRADE III. LOCATION AS DESIGNATED AS SHOWN.
5. TRANSIPAD (ITEMS 91 AND 92) TO BE INSTALLED UNDER TRANSISTORS TO-5 AND TO-18 PRIOR TO INSTALLING ON BOARD.
6. ALL COMPONENTS TO BE MOUNTED IN ACCORDANCE WITH DATARAM QC SPEC. 20C2000.
7. COMPONENT LEAD TRIM AND SOLDER BUILD-UP AS NOTED
8. RAISE RESISTORS OVER ½ WATT OFF BOARD TO .360 MAX HEIGHT.
9. ITEM 102 TO BE INSTALLED AFTER ITEM 89.
10. WIRE-WRAP USING #30 AWG (PN24305) A TO B, C TO D, E TO F, V TO W, P TO R & J TO H.
11. ITEM 103 TO BE INSTALLED BETWEEN P.C. BOARD & EXTRACTOR.



SECTION A-A SCALE 2:1
TYP DIODE MODULE MOUNTING

DETAIL B SCALE 2:1
TYP PIN ORIENTATION FOR INTEGRATED CIRCUITS (14 AND 16 PINS) TM'S, MHQ'S AND TBI.

NEXT ASSY	USED ON
	DR-111
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON:
FRACTIONS ± DECIMALS xx ± .02 xxx ± .010 ANGLES ±
MATERIAL:

DRAWN	M. BOCK	DATE 3-20-75
CHECKED	P. PFEIFFER	3-25-75
ENGR		
APPROVED		4/22/75

DATARAM CORPORATION
CRANBURY NEW JERSEY

ASSEMBLY
DR-111 MEMORY SYSTEM
16K x 16 BITS

SIZE	CODE IDENT NO	DRAWING NO	REV
D	50473	61101	F

SCALE ½ SHEET 1 OF 2

500033 A A

WHEN REFERRING TO THIS DRAWING STATE DRAWING NO., APPLICABLE REVISION LETTER IF ANY, AND DATE

REVISIONS				
SYM.	SHEET	DESCRIPTION	APPROV.	DATE
NC		REL TO PRODUCTION	BP	3-25-75
A		Released to DRC Production	GYW	4-21-75
B		ECN 571	GYW	9-17-75
C		ECN 610, 610A	GYW	9-11-75
D		ECN 639A	GYW	9-17-75
E		ECN 657A		11-11-75
F		ECN 697	GYW	12-31-75
G		ECN 756	GYW	4-30-75

DRAWN	DATE 3-25-75	TITLE: BILL OF MATERIAL MEMORY SYSTEM 16K X 16 BITS DR 111
CHECKED RD	DATE 3-25-75	
	DATE 3-25-75	DATARAM CORPORATION PRINCETON NEW JERSEY
APPROVED	DATE 4/23/75	DWG. NO. B/M A 61101 SHEET 1 OF 8
		REV. G

ITEM NO.	QTY.	PART NUMBER	DESCRIPTION	SUGGESTED MANUFACTURER	REFERENCE NOTES
1	8	10213	RESISTOR, FILM, 1/10 watt, 2.74 K, 1%		R21, 23,49,51,99,
					101,127,129
2	1	10210	RESISTOR, FILM, 1/10 WATT, 1K, 1%		R177
3	2	10219	RESISTOR, FILM, 1/10, WATT, 562 OHMS, 1%		R168,172
4	1	10226	RESISTOR ,FILM, 1/10 WATT 422 OHMS, 1%		R173
5	18	10201	RESISTOR, FILM, 1/10, WATT, 10 OHMS, 1%		R22,24,50,52,98
					100,126,128,
					142 - 146,149-153
6			NOT USED		
7			NOT USED		
8	2	10122	RESISTOR, CC, 1/4 WATT, 10K 5%		R67,69
9	6	10121	RESISTOR, CC, 1/4 WATT, 4.7 K, 5%		R57,58,59,64,65,
					75
10	2	10119	RESISTOR,CC,1/4 WATT, 3.3K, 5%		R162,169
11	1	10118	RESISTOR,CC,1/4 WATT, 2.2K ,5 %		R73
12	36	10113	RESISTOR,CC,1/4 WATT, 1.0K 5%		R1-4, 13,15,16,18
					29-32,41,43,44,
					46,60,62,78-81,90
					92,93,95,106-109
					118,120,121,123,
					178,179
13	6	10111	RESISTOR,CC,1/4 WATT ,470 OHMS, 5%		R63,74,138-141,
14			NOT USED		

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

DATARAM CORPORATION
PRINCETON NEW JERSEY

DWG. NO. B/M A 61101
SHEET 2 OF 8

REV. G

TITLE: B/M MEMORY SYSTEM 16K X 16 BITS (DR-111)

ITEM NO.	QTY.	PART NUMBER	DESCRIPTION	SUGGESTED MANUFACTURER	REFERENCE NOTES
15	7	10164	RESISTOR, CC, 1/4 WATT, 330 OHMS, 5%		R61,71,72,77, 167
					175, 176
16	1	10108	RESISTOR, CC, 1/4 WATT, 220 OHMS, 5%		R68
17	4	10105	RESISTOR, CC, 1/4 WATT, 100 OHMS, 5%		R155,156, 171,180
18	6	10102	RESISTOR, CC, 1/4 WATT, 47 OHMS, 5%		R134-137,
					166,170
19	16	10109	RESISTOR, CC, 1/4 WATT, 270 OHMS, 5%		R12,14, 17, 19,
					40,42,45,47,89,
					91,94,96,117,119
					122,124
20	1	10159	RESISTOR, CC 1/4 WATT, 75 OHMS, 5%		R165
21	1	10233	RESISTOR, FILM, 1/10 WATT, 46.4 OHMS, 1%		R181
22			NOT USED		
23	1	10402	RESISTOR, VARIABLE 10K		R76
24			NOT USED		
25	3		RESISTOR, 1/4 WATT, SELECT AT TEST		R154,157,174
26	2		RESISTOR, 1/4 WATT, SELECT AT TEST		R66, 70
27			NOT USED		
28	1	10165	RESISTOR, CC, 1/2 WATT, 390 OHMS, 5%		R148
29	3	10161	RESISTOR, CC, 1/2 WATT, 220 OHMS, 5%		R160,161,147
30	16	10160	RESISTOR, CC, 1/2 WATT, 39 OHMS, 5%		R7-10,35-38,
					84-87,112-115

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

DATARAM CORPORATION
PRINCETON NEW JERSEY

DWG. NO. B/M A 61101
SHEET 3 OF 8

REV. G

DRAWING NO. 11402

ITEM NO.	QTY.	PART NUMBER	DESCRIPTION	SUGGESTED MANUFACTURER	REFERENCE NOTES
31			NOT USED		
32	2	10166	RESISTOR, CC. 2 WATT, 180 OHMS , 5%		R163,164
33	16	10333	RESISTOR, WW, NI, 5 WATT, 12 OHMS, 1%		R5,6,11,20,33,34
					39,48,82,83,88,97
					110,111,116,125
34	2	10321	RESISTOR WW, NI, 2.5 WATT, 7.5 OHMS , 1%		R158, 159
35			NOT USED		
36			NOT USED		
37	7	11903	RESISTOR, MODULE, 470 OHMS, 5%		RM5-7, 14-17
38	8	11801	RESISTOR MODULE, 100 OHMS, 5%		RM1-4, 18-21
39	6	11901	RESISTOR MODULE, 47 OHMS, 5%		RM8-13
40			NOT USED		
41			NOT USED		
42	16	12315	CAPACITOR, CERAMIC, .01uf, 20%		C1,3,18,20,23,25
					39,41,66,68,82,84
					87,89,103,105
43	2	12517	CAPACITOR, SILVER MICA , 220 pf, 5%		C51, 111

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

ITEM NO.	QTY.	PART NUMBER	DESCRIPTION	SUGGESTED MANUFACTURER	REFERENCE NOTES
44	14	12513	CAPACITOR, SILVER MICA, 100 pf, 5%		C8,10,29,31,47,
					52,53,55,72,74
					93,95,54,46
45	1		CAPACITOR, SILVER MICA, S.A.T. 5%		C49
46	17	12516	CAPACITOR, SILVER MICA, 47 pf, 5%		C12-15,33-36,
					76-79,97-100
					109
47	1	12515	CAPACITOR, SILVER MICA, 22pf, 5%		C63
48	3	12522	CAPACITOR, SILVER MICA, 10pf, 5%		C48,62,64
49	1	12512	CAPACITOR, SILVER MICA, 820 Pf, 5%		C110
50	18	12102	CAPACITOR, TANTALUM, 15uf, 20 VOLTS		C5-7,19,26-28,40
					67,70,71,83,88,91
					92,104,107,112,
51	34	12105	CAPACITOR, TANTALUM, 4.7uf, 10 VOLTS		C2,4,9,17,21,22,
					24,30,38,42-45,50
					56-61,65,69,73,81
					85,86,90,94,102,
					106,108,113,114,
					115
52			NOT USED		
53	18	14204	TRANSFORMER, PULSE 10mh, QUAD		TM1-18
54	2	14502	INDUCTOR 22 uh		L2,3
55			NOT USED		

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REV. G

BRUNING 40-105 11402

ITEM NO.	QTY.	PART NUMBER	DESCRIPTION	SUGGESTED MANUFACTURER	REFERENCE NOTES
56	13	20401	TRANSISTOR, QUAD, DIP		MHQ1-13
57	22	20202	TRANSISTOR, NPN, CORE DRIVER, 2N3725		Q1-8,10-22,28
58	10	20203	TRANSISTOR, PNP, 2N2905		Q23-27,29,30,33-
					35
59	5	20104	TRANSISTOR , NPN, 2N2369A		Q9,31,32,26,37
60			NOT USED		
61	1	18205	DIODE, ZENER, 5.1 VOLT , 1N751A		CR 115
62			NOT USED		
63	115	18101	DIODE, SILICON, HIGH CONDUCTANCE		CR1-114, 116
64	8	18307	DIODE MODULE, COMMON ANODE		CRM1,2,4,6,8,10,
					11,12
65	4	18308	DIODE MODULE, COMMON CATHODE		CRM3,5,7,9,
66			NOT USED		
67	1	10506	THERMISTOR, 1K		RT1
68			NOT USED		
69	7	16401	I.C., QUAD 2 I/P AND GATE, 74H00		Z28,32,38,43,54,
					55,56
70	3	16402	I.C., HEX INVERTER, 74H04		Z29,31,41
71	3	16403	I.C., QUAD 2 I/P AND GATE, 74H08		Z33,40,52
72	2	16404	I.C., TRIPLE 3 I/P NAND GATE, 74H10		Z35,39
73			NOT USED		
74	1	16310	I.C., DUAL 4 I/P NAND GATE, 7440		Z27
75	1	16333	I.C., 8 I/P NAND GATE, 7430		Z26

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

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DWG. NO. B/M A61101
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REV. G

BRUNING 40-105 11402

TITLE: B/M MEMORY SYSTEM FOR X 16 BITS BR-11

ITEM NO.	QTY.	PART NUMBER	DESCRIPTION	SUGGESTED MANUFACTURER	REFERENCE NOTES
76	2	16309	I.C,,QUAD 2 I/P NAND GATE, 7438		Z53,58
77	1	16512	I.C. EXP. DUAL 2 I/P AND OR GATE 74S51		Z37
78			NOT USED		
79	10	16407	I.C.,DUAL D-TYPE FLIP-FLOPS ,74H74		Z5,6,11,12,30,34
					59,60,65,66
80	4	16314	I.C.,QUAD D LATCH, 7475		Z21,22,23,24
81	3	16326	I.C.,DUAL MONOSTABLE MULTIVIBRATOR, 74123		Z36,42,57
82	9	16312	I.C.,BCD TO DECIMAL DECODER, 74145		Z25,44-51,
83	8	16602	I.C. DUAL SENSE AMPLIFIER, 75234		Z8,10,14,16,62,
					64,68,70
84	8	16607	I.C.,DUAL PERIPHERAL OR DRIVER, 75453		Z7,9,13,15,61,63
					67,69
85	4	16334	I.C.,HEX UNIFIED BUS RECEIVER,8837		Z17-20
86	4	16335	I.C.,QUAD UNIFIED BUS TRANSCEIVER ,8838		Z1-4
87	1	42649	STIFFENER, CIRCUIT CARD		
88	8	22214	BEAD PIN		P2,P3
89	1	23003	I.C. SOCKET, 16 PIN		TB1
90	115	22801	CONTACT, FEMALE, REAR ENTRY		
91	32	27305	PAD, TRANSISTOR, TO-5		
92	5	27316	PAD, TRANSISTOR, TO-18		
93	19	22601	CONTACT, MALE		

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

DATARAM CORPORATION
PRINCETON NEW JERSEY

DWG. NO. B/MA 61101
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REV. G

BRUNING 40-105 11402

TITLE: B/M MEMORY SYSTEM 16K X 16 BITS DR-111

ITEM NO.	QTY.	PART NUMBER	DESCRIPTION	SUGGESTED MANUFACTURER	REFERENCE NOTES
94	2	42650	HANDLE-INSERTOR, EXTRACTOR		
95	2	26306	SCREW ,2-56 X 5/16 LG.		
96	2	26107	NUT,HEX # 2 SELF LOCKING		
97	2	42651	SPACER, HANDLE MOUNT		
98	5	27002	SCREW,2-56 X 1/4 LG,NYLON		
99	1	50449	ASSEMBLY, CORE STACK		
100	10	26105	NUT, NEX 4-40, NYLON		
101	1	40530	PRINTED CIRCUIT BOARD		
102	1	23009	ADAPTER PLUG, 16 PIN		
103	2	26212	WASHER, BELLEVILLE SPRING		

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

DATARAM CORPORATION
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REV. G

BRUNING 40-105 11402

DATABAM CODE MEMORY